Schematic Package Supplement to

Kangaroo™

Operation, Maintenance and Service Manual

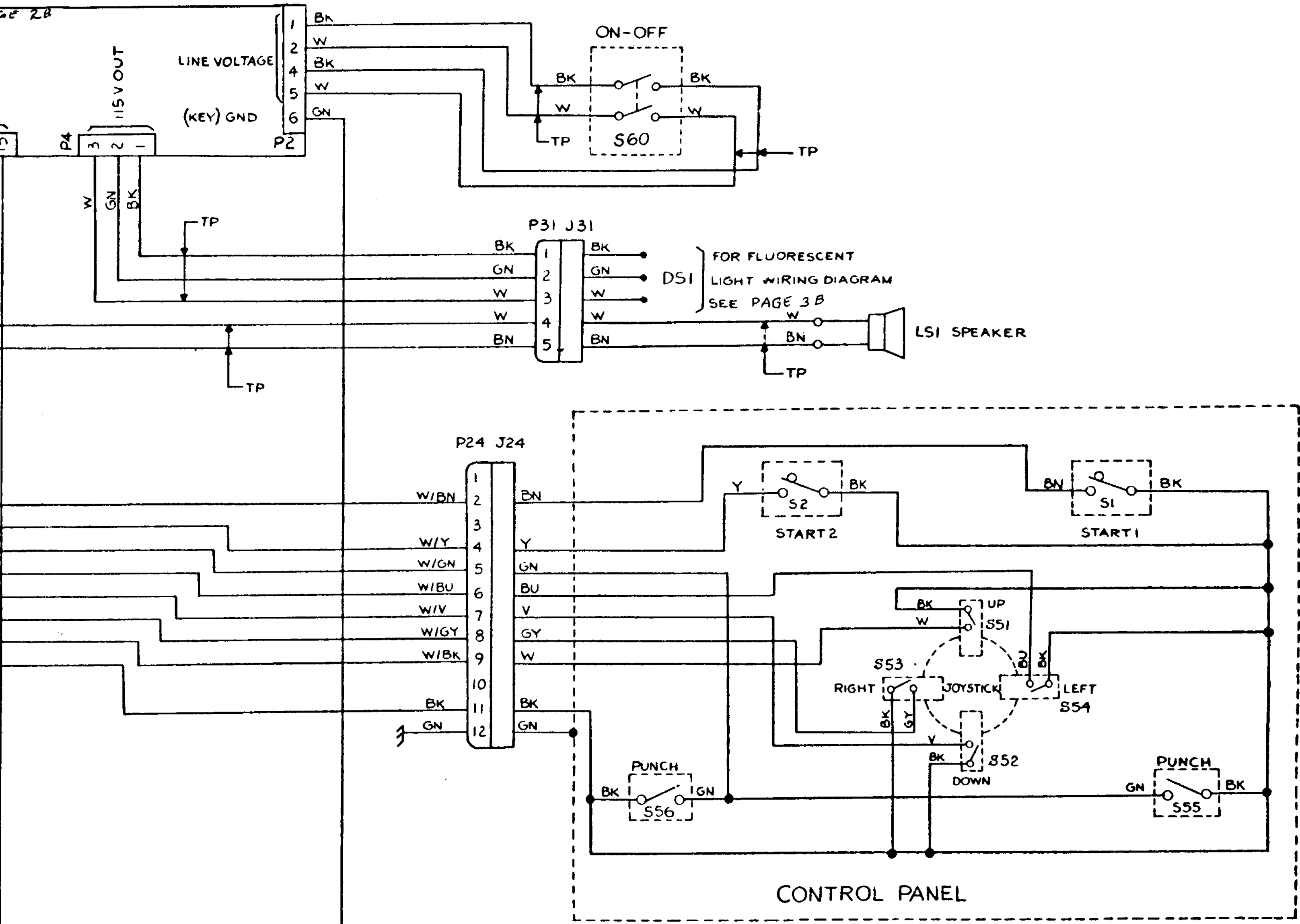
NOTE
This staple temporarily holds the schematic package together. Remove the staple before using the schematics.

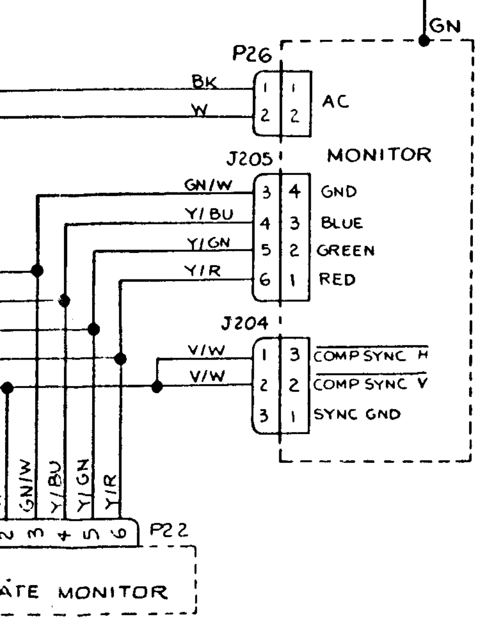
ATARI®
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7L

SP-204 Sheet 1A
3rd printing

Table of Contents

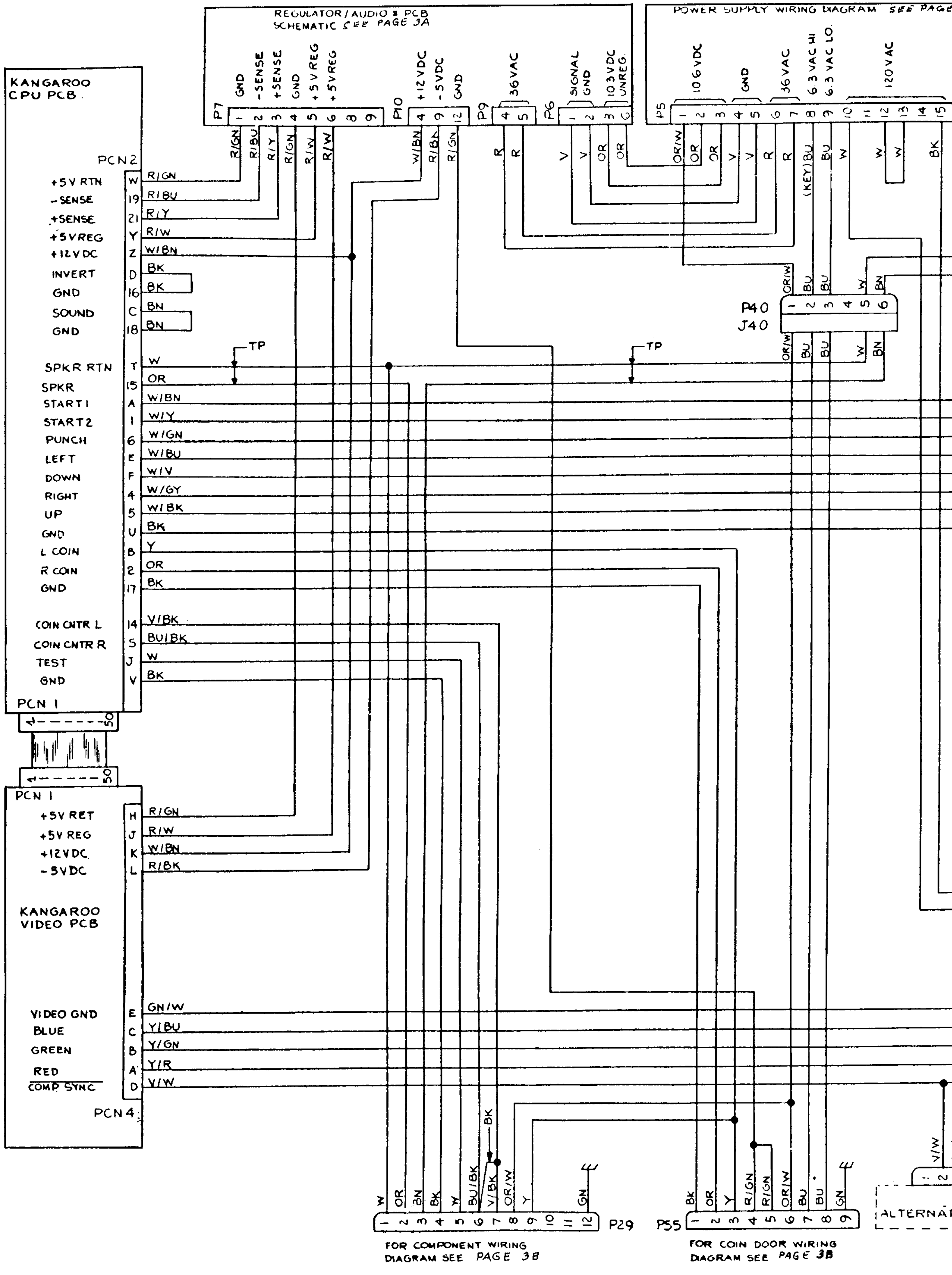




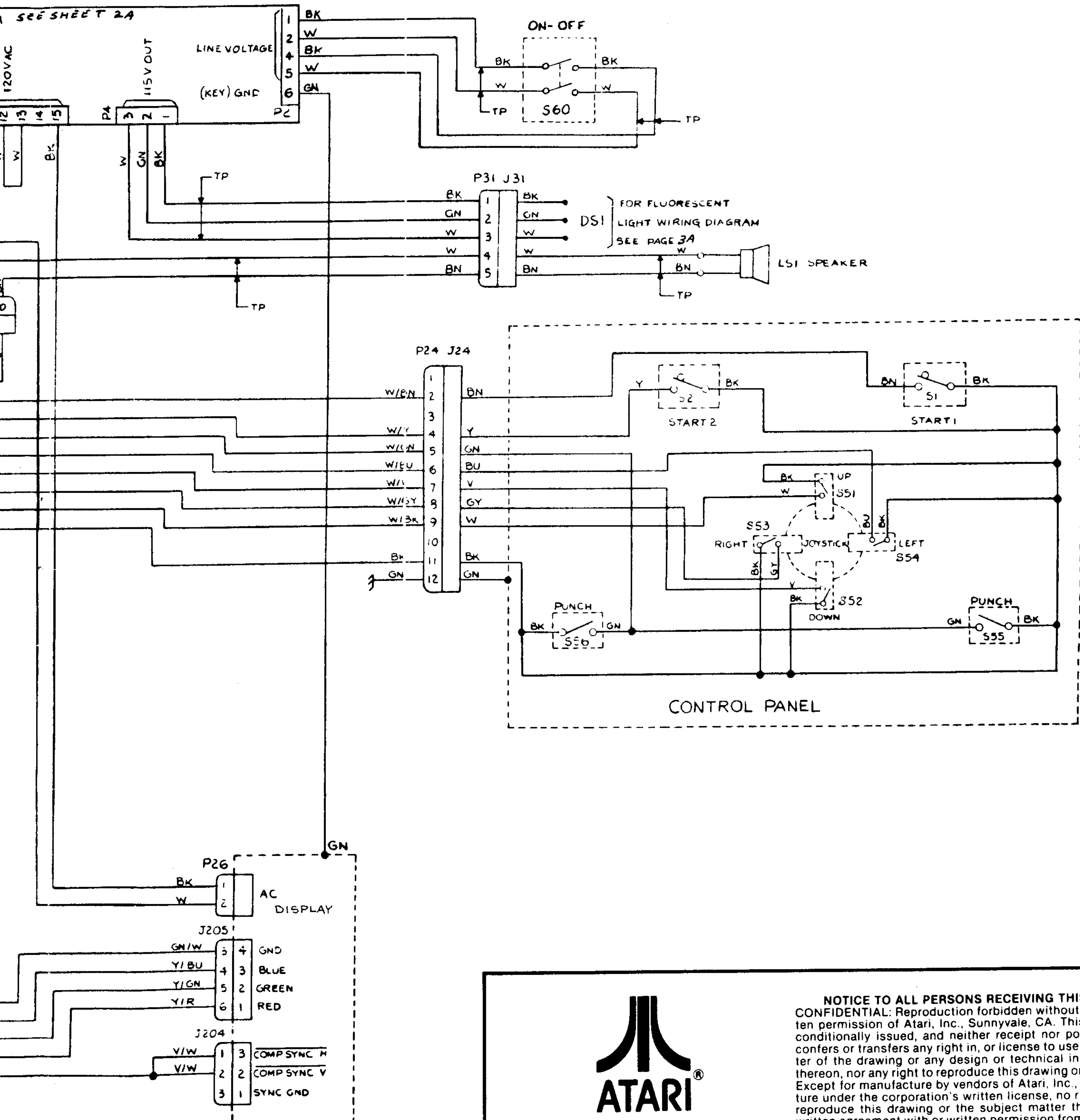
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Kangaroo Upright Game Wiring Diagram

SP-204 Sheet 1B
3rd printing



REGULATOR / AUDIO II PCB SCHEMATIC SEE PAGE 3A
POWER SUPPLY WIRING DIAGRAM SEE PAGE
KANGAROO CPU PCB
PCN 2
+5V RTN
-SENSE
+SENSE
+5V REG
+12VDC
INVERT
GND
SOUND
GND
SPKR RTN
SPKR
START 1
START 2
PUNCH
LEFT
DOWN
RIGHT
UP
GND
L COIN
R COIN
GND
COIN CNTR L
COIN CNTR R
TEST
GND
PCN 1
KANGAROO VIDEO PCB
+5V RET
+5V REG
+12VDC
-5VDC
VIDEO GND
BLUE
GREEN
RED
COMP SYNC
PCN 4
P7
P10
P9
P6
P5
GND
+5V REG
+12VDC
-5VDC
36VAC
SIGNAL GND
103VDC UNREG.
106VDC
6.3 VAC HI
6.3 VAC LO.
120VAC
(KEY)
P40
J40
TP
P29
P55
ALTERNA
FOR COMPONENT WIRING DIAGRAM SEE PAGE 3B
FOR COIN DOOR WIRING DIAGRAM SEE PAGE 3B



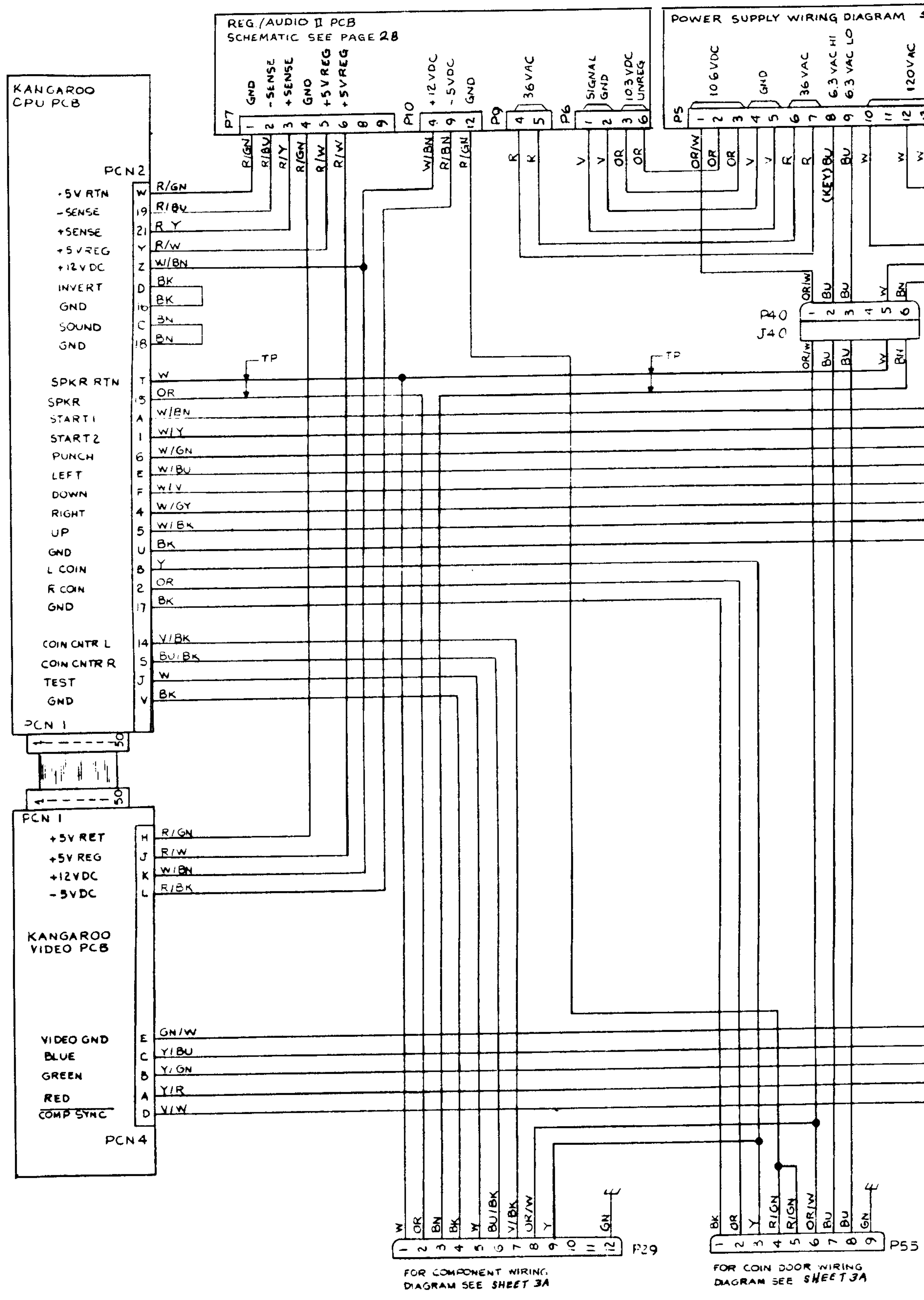
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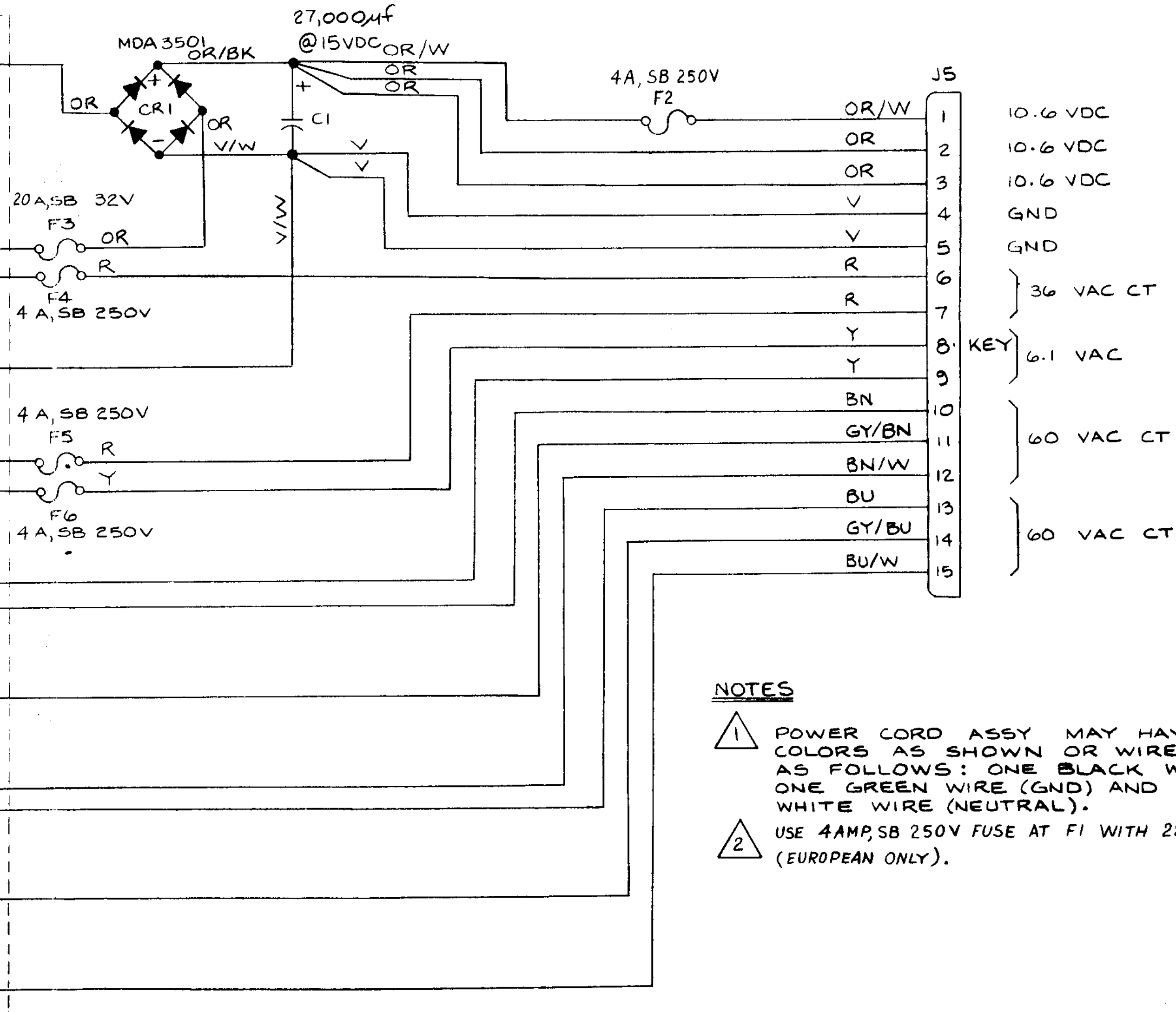
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Ireland-Built
Kangaroo Game Wiring Diagram

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REG./AUDIO II PCB
SCHEMATIC SEE PAGE 28
POWER SUPPLY WIRING DIAGRAM
KANGAROO CPU PCB
PCN2
+5V RTN
-SENSE
+SENSE
+5VREG
+12VDC
INVERT
GND
SOUND
GND
SPKR RTN
SPKR
START 1
START 2
PUNCH
LEFT
DOWN
RIGHT
UP
GND
L COIN
R COIN
GND
COIN CNTR L
COIN CNTR R
TEST
GND
PCN 1
KANGAROO VIDEO PCB
+5V RET
+5V REG
+12VDC
-5VDC
VIDEO GND
BLUE
GREEN
RED
COMP SYNC
PCN4
P7
P10
P9
P6
P5
P40
J40
P29
P55
TP
GND
-SENSE
+SENSE
GND
+5VREG
+5VREG
+12VDC
-5VDC
GND
36VAC
SIGNAL GND
103VDC UNREG
106VDC
GND
36VAC
6.3 VAC HI
6.3 VAC LO
120VAC
(KEY)BU
FOR COMPONENT WIRING DIAGRAM SEE SHEET 3A
FOR COIN DOOR WIRING DIAGRAM SEE SHEET 3A



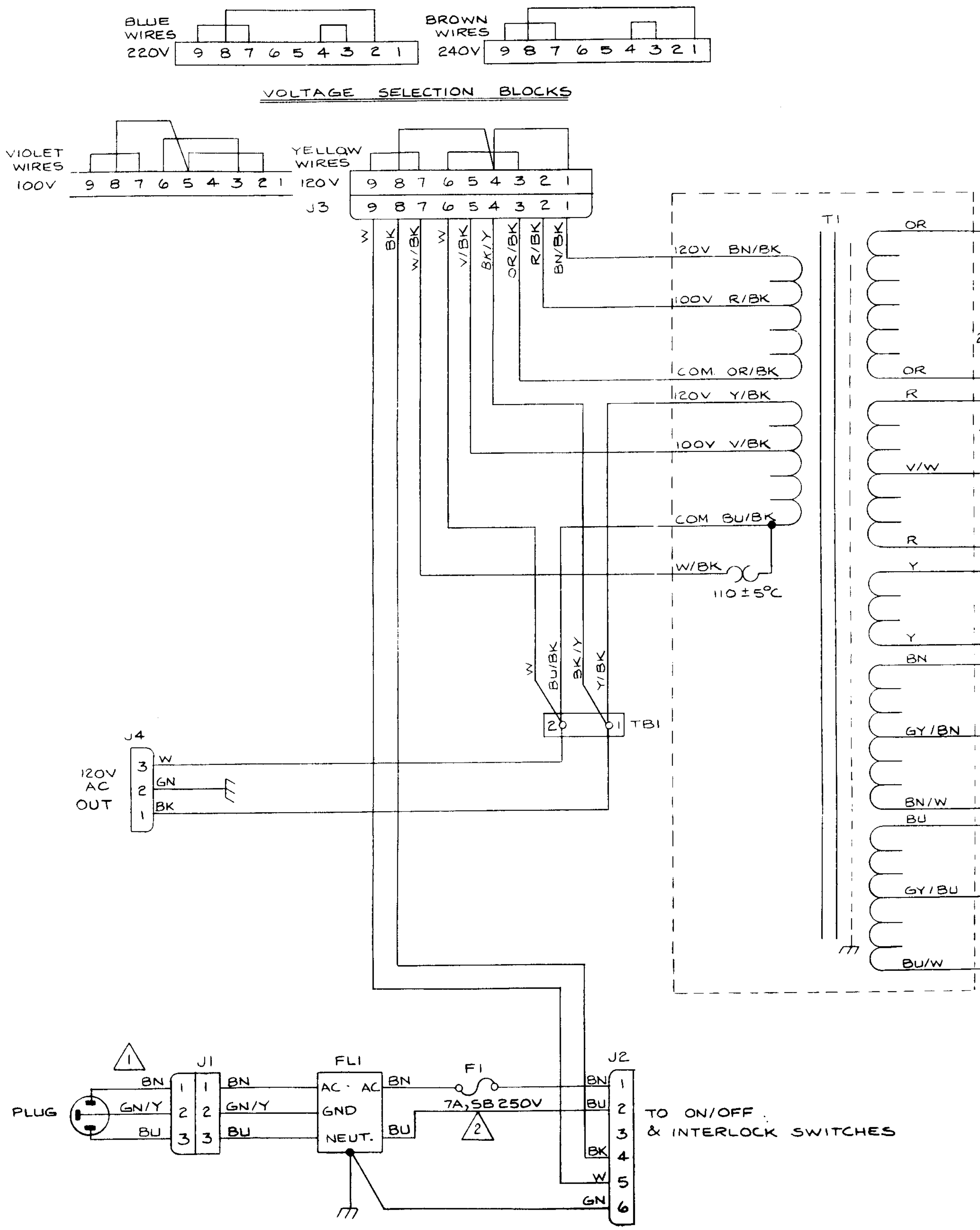
NOTES

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
2. *USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).*

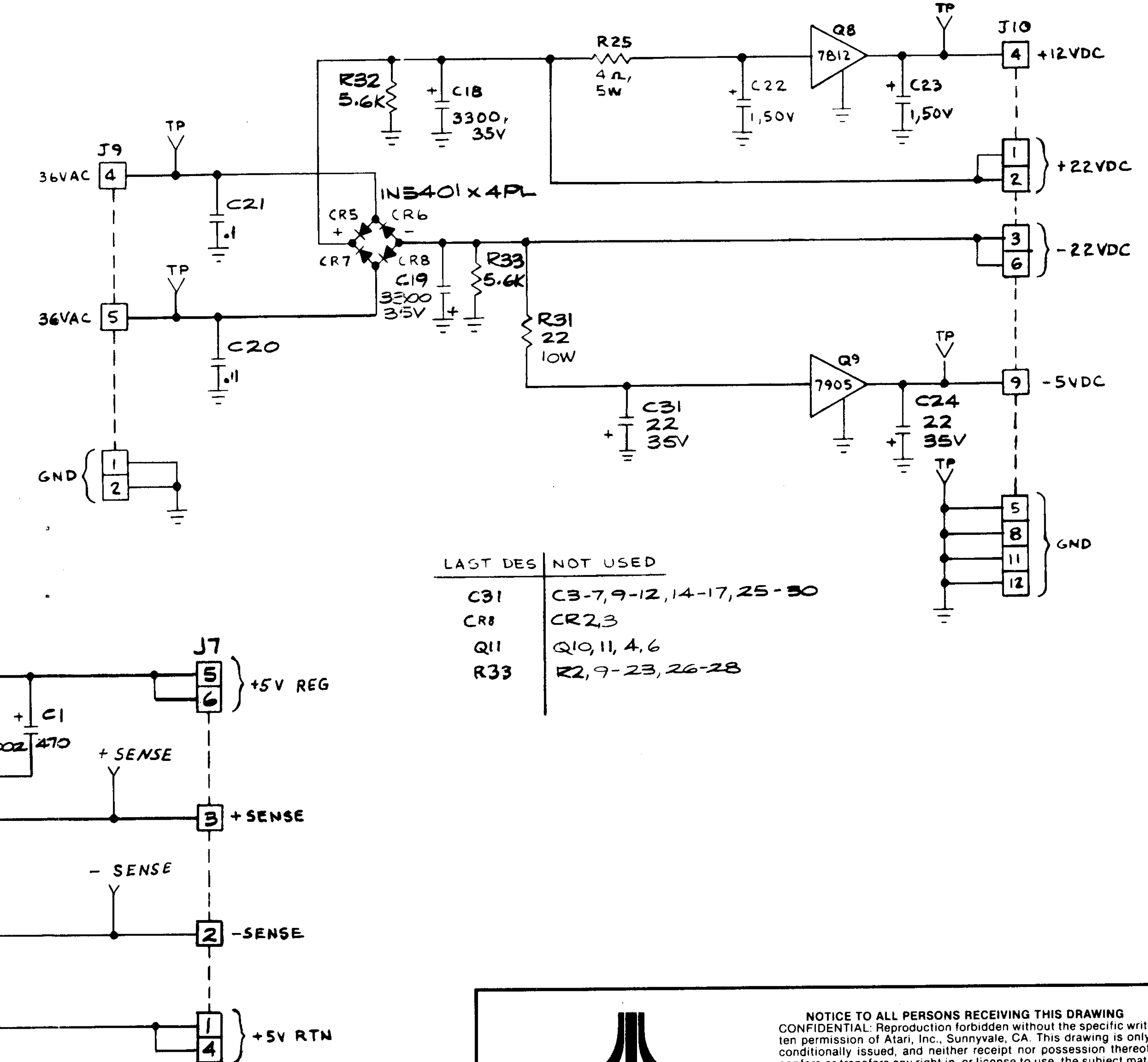
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Kangaroo Power Supply

SP-204 Sheet 2B
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BLUE WIRES 220V
9 8 7 6 5 4 3 2 1
BROWN WIRES 240V
9 8 7 6 5 4 3 2 1
VOLTAGE SELECTION BLOCKS
VIOLET WIRES 100V
YELLOW WIRES 120V
J3
W
BK
W/BK
V/BK
BK/Y
OR/BK
R/BK
BN/BK
T1
120V BN/BK
100V R/BK
COM. OR/BK
120V Y/BK
100V V/BK
COM BU/BK
W/BK
110 ± 5°C
OR
R
V/W
Y
BN
GY/BN
BN/W
BU
GY/BU
BU/W
BU/BK
TB1
J4
120V AC OUT
GN
PLUG
GN/Y
J1
FL1
AC · AC
GND
NEUT.
F1
7A, SB 250V
J2
TO ON/OFF & INTERLOCK SWITCHES



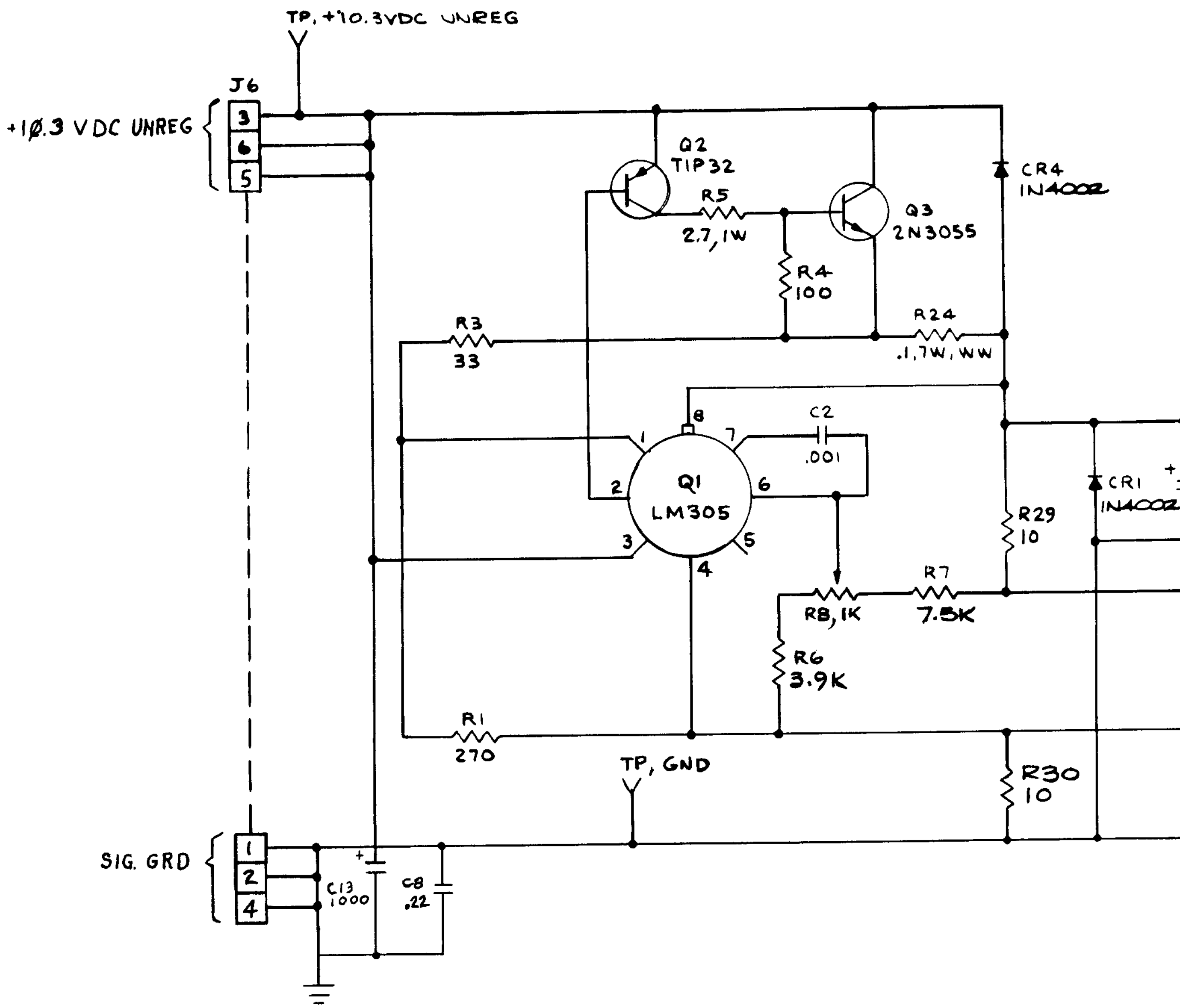
LAST DES	NOT USED
C31	C3-7, 9-12, 14-17, 25-30
CR8	CR2,3
Q11	Q10, 11, 4, 6
R33	R2, 9-23, 26-28

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Kangaroo Reg./Audio II PCB Schematic Diagram

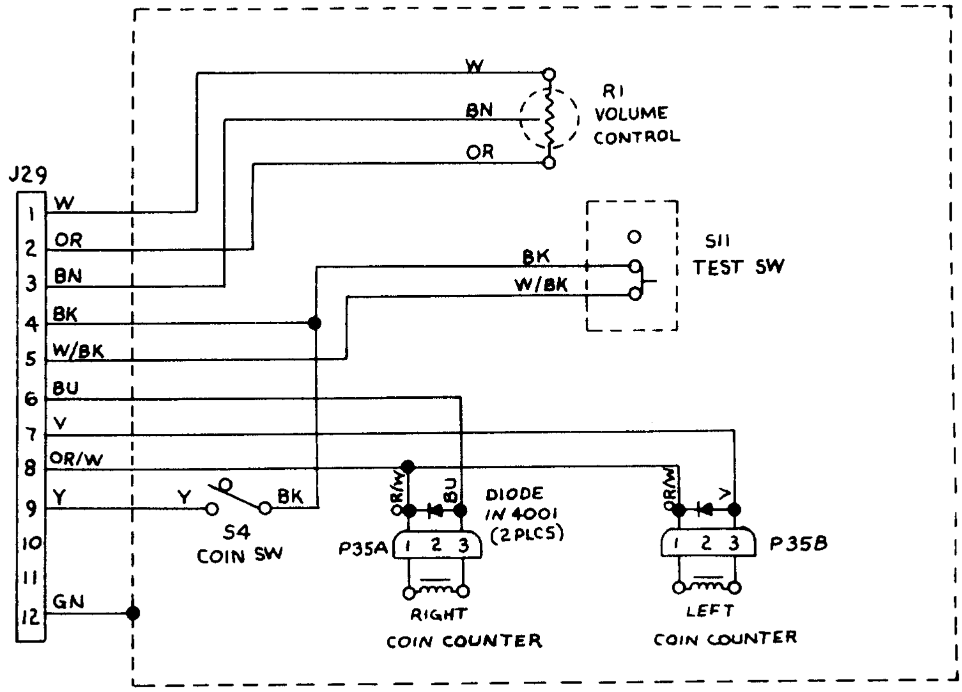
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3rd printing

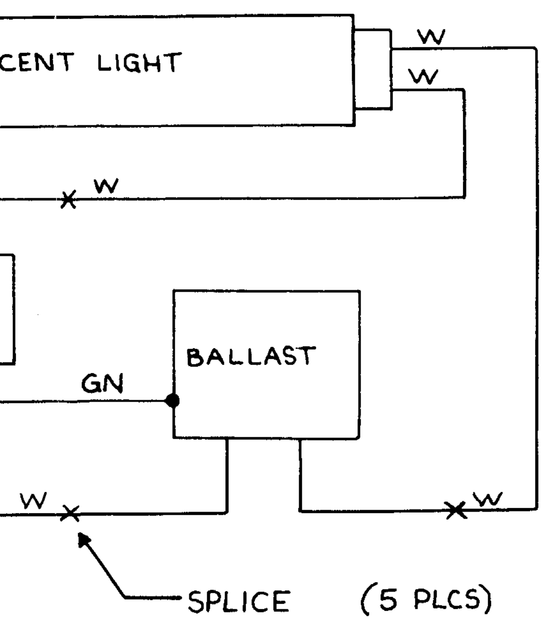


TP, +10.3VDC UNREG
J6
+1Ø.3 VDC UNREG
3
6
5
Q2
TIP32
R5
2.7, 1W
Q3
2N3055
CR4
IN4002
R4
100
R3
33
R24
.1, 7W, WW
8
7
C2
.001
1
2
Q1
LM305
6
3
5
4
CR1
IN4002
R29
10
R7
7.5K
R8, 1K
R6
3.9K
R1
270
TP, GND
R30
10
SIG. GRD
1
2
4
C13
1000
C8
.22

Utility Panel Wiring Diagram



Speaker Wiring Diagram



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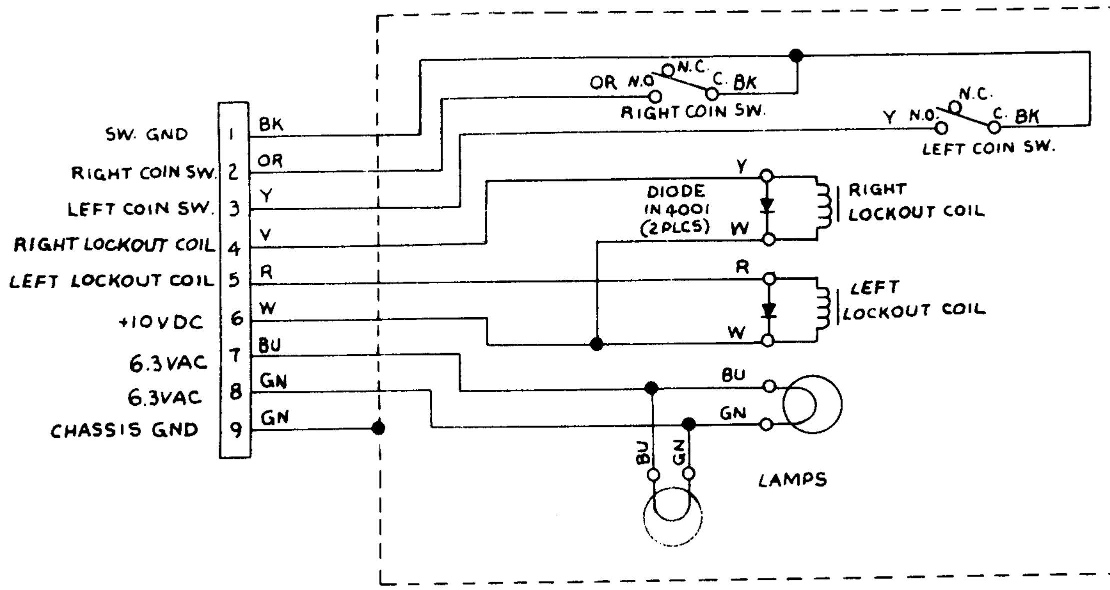
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Kangaroo Game Wiring Interfaces

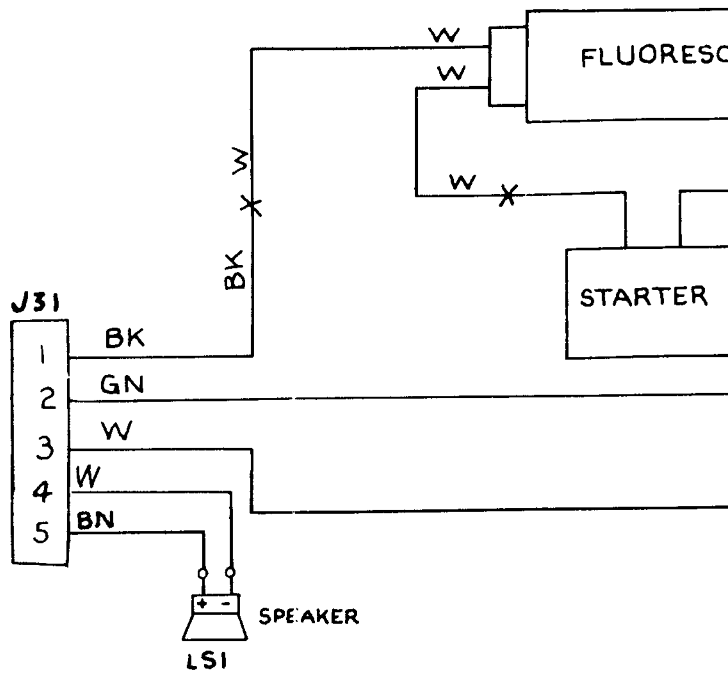
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Coin Door Wiring Diagram

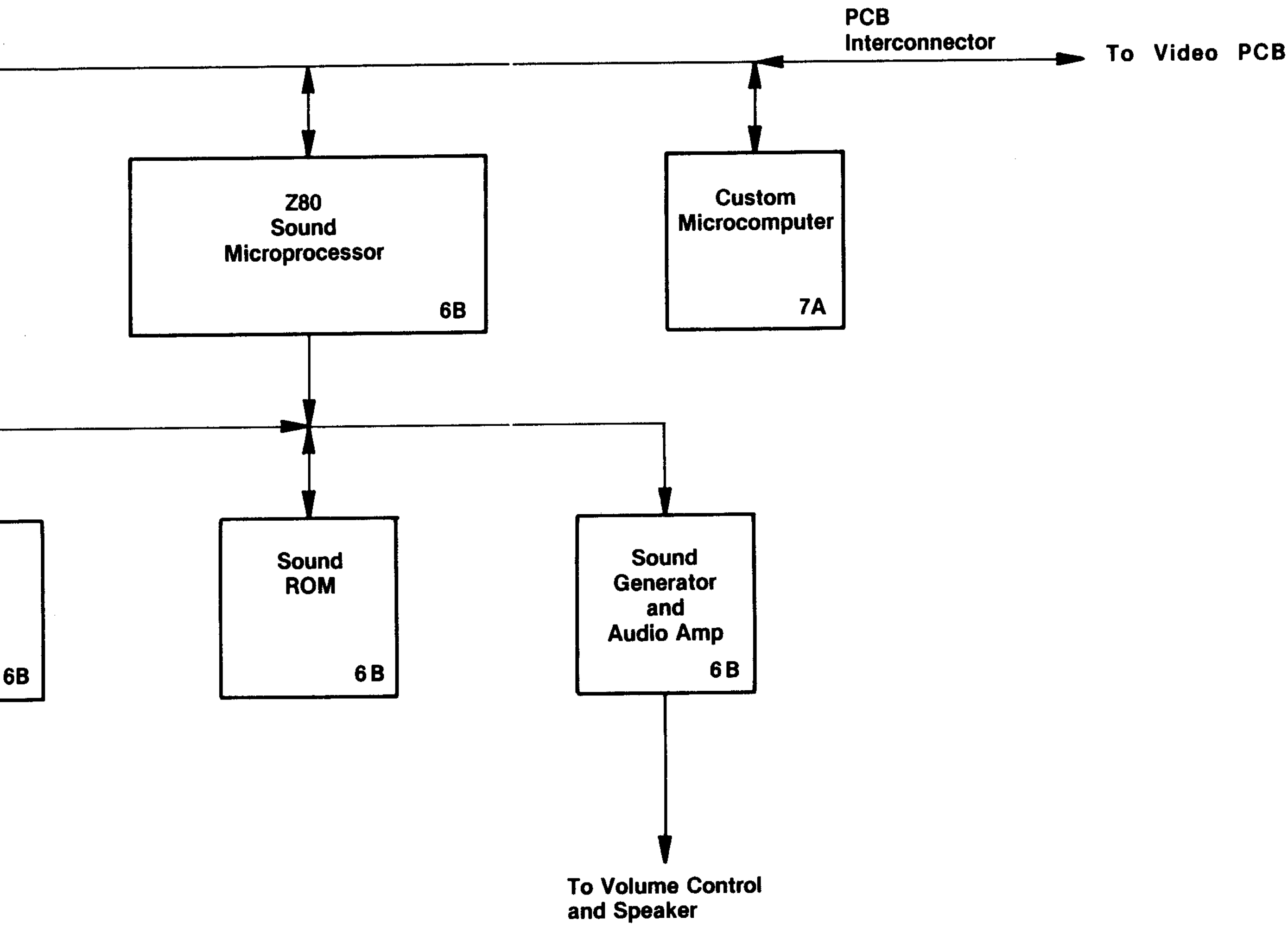


Fluorescent Light and



NOTE

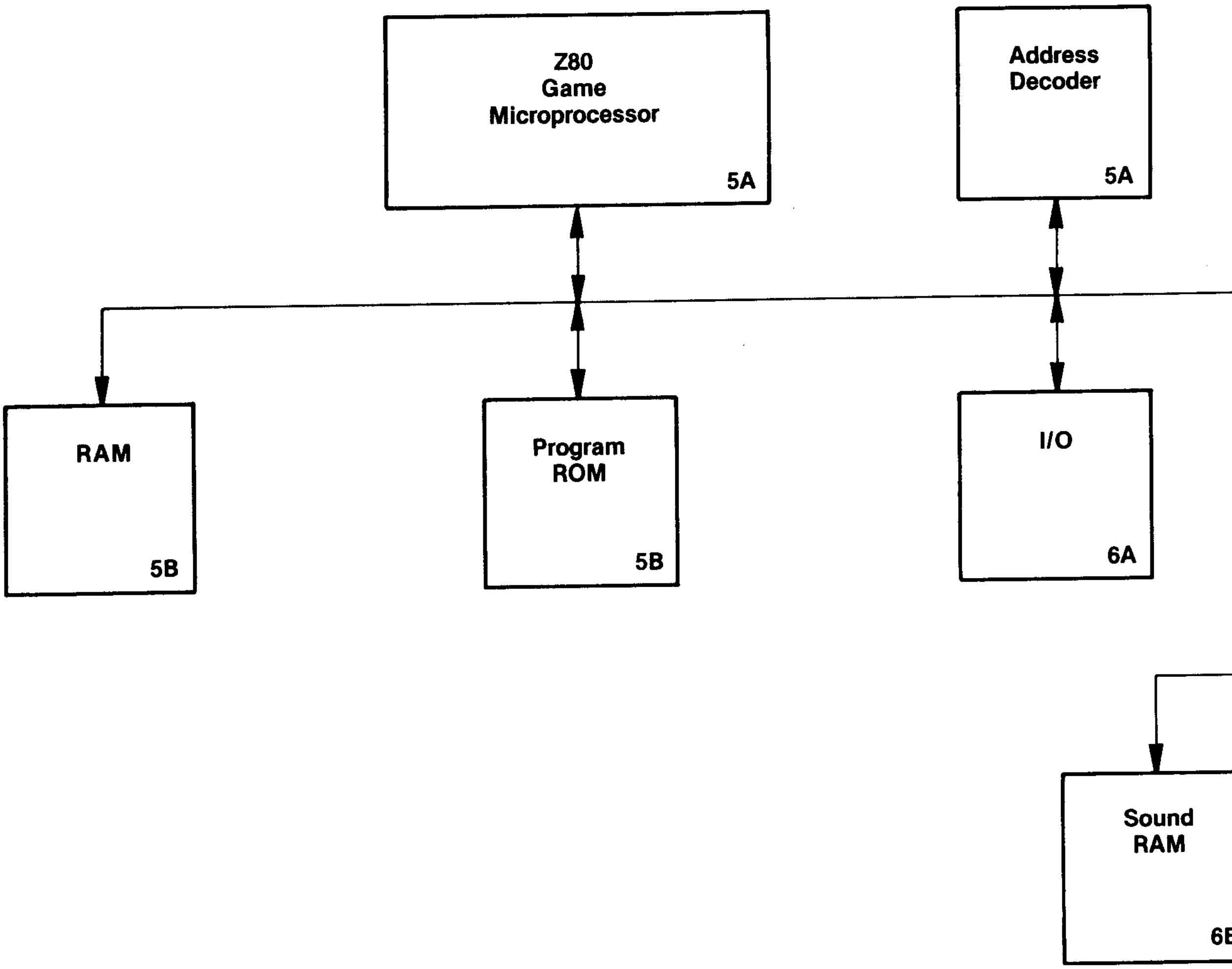
The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



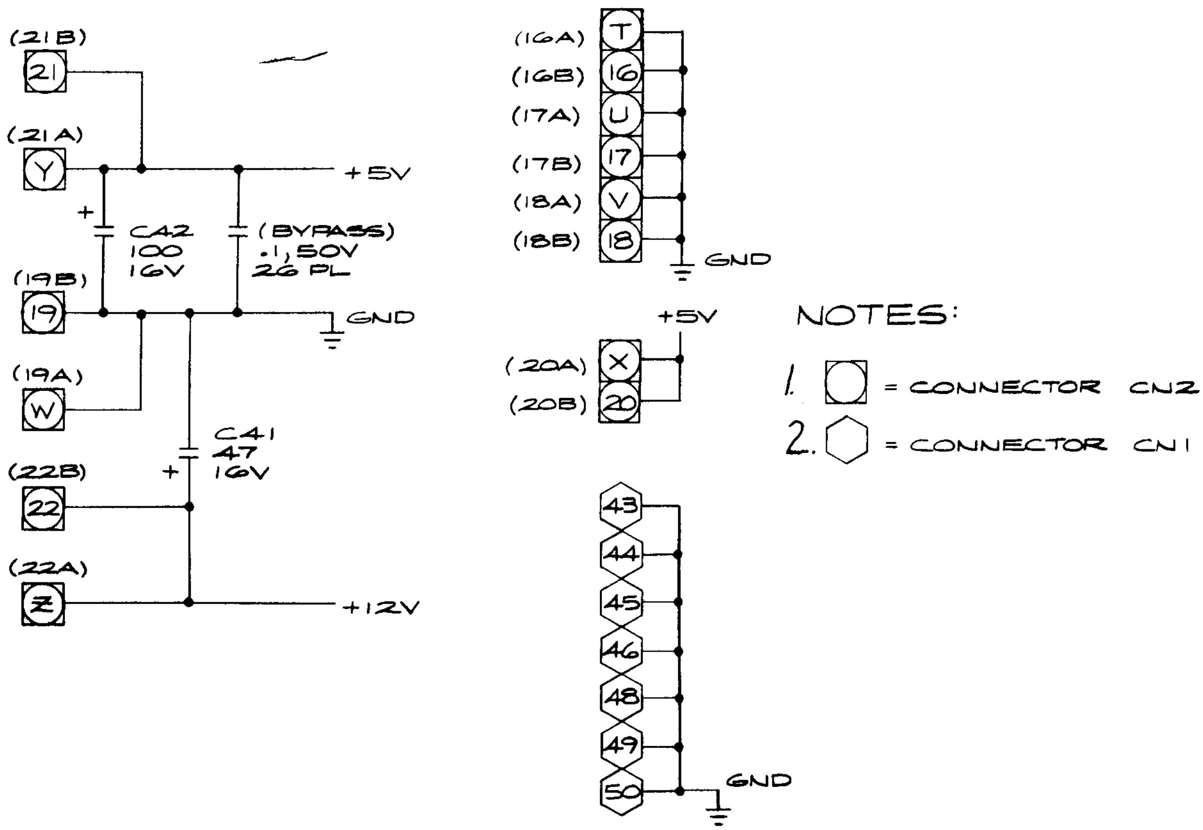
Kangaroo CPU PCB Schematic Diagram

SP-204 Sheet 4A
3rd printing

Block Diagram (CPU PCB)



CPU Power Input



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Kangaroo CPU PCB Schematic Diagram

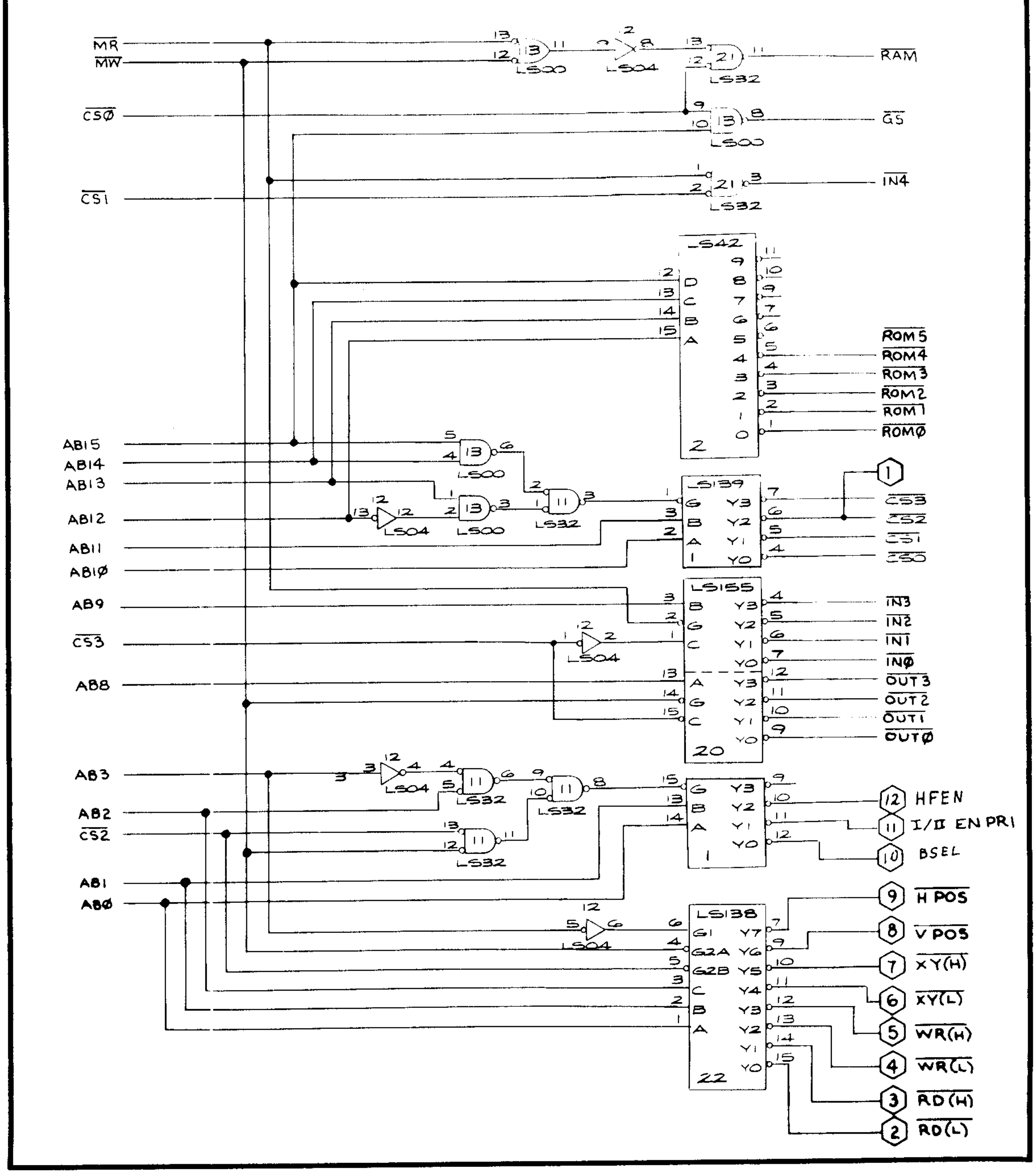
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Memory Map

HEXA-DECIMAL ADDRESS	R/W	DATA								FUNCTION
		D7	D6	D5	D4	D3	D2	D1	D0	
Game Microprocessor Memory Space (IC15)										
0000-5FFF	R	D	D	D	D	D	D	D	D	Z80 24K Program ROM
E000-E3FF	R/W	D	D	D	D	D	D	D	D	1K Working RAM
E400	R	D	D	D	D	D	D	D	D	Option Switch
E800	W	D	D	D	D	D	D	D	D	Low Byte ⎤ Start Address of Data in Picture
E801	W	D	D	D	D	D	D	D	D	High Byte ⎦ ROM for DMA
E802	W	D	D	D	D	D	D	D	D	Low Byte ⎤ Start Address in Bit Map RAM (where
E803	W	D	D	D	D	D	D	D	D	High Byte ⎦ picture is to be written) During DMA
E804	W	D	D	D	D	D	D	D	D	Low Byte ⎤ Picture Size for DMA
E805	W	D	D	D	D	D	D	D	D	High Byte ⎦ and DMA Start
E806	W	D	D	D	D	D	D	D	D	Vertical Start Address in Bit Map
E807	W	D	D	D	D	D	D	D	D	Horizontal Start Address in Bit Map
E808	W							D	D	Bank Select Latch
E809	W			D	D	D	D	D	D	A & B Bit Map Control Latch (A = playfield, B = motion)
E80A				D	D	D	D	D	D	Color-Shading Latch
EC00	W	D	D	D	D	D	D	D	D	Sound DATA to Sound Microprocessor
EC00	R								D	Utility Coin Switch
EC00	R							D		1 Player Start
EC00	R						D			2 Player Start
EC00	R					D				Left Coin Input
EC00	R				D					Right Coin Input
ED00	W								D	Coin Counter 1
ED00	W							D		Coin Counter 2 (European games)
ED00	R								D	Player 1 Right
ED00	R							D		Player 1 Left
ED00	R						D			Player 1 Up
ED00	R					D				Player 1 Down
ED00	R				D					Player 1 Punch
EE00	R								D	Player 2 Right
EE00	R							D		Player 2 Left
EE00	R						D			Player 2 Up
EE00	R					D				Player 2 Down
EE00	R				D					Player 2 Punch
EFXX	W					D	D	D	D	Output to Custom Microcomputer
EFXX	R					D	D	D	D	Input from Custom Microcomputer
Sound Microprocessor Memory Space (IC34)										
0000-0FFF	R	D	D	D	D	D	D	D	D	4K Program ROM
4000-43FF	R/W	D	D	D	D	D	D	D	D	1K Working RAM
6000	R	D	D	D	D	D	D	D	D	Read DATA from Game Microprocessor
7000	W	D	D	D	D	D	D	D	D	Write to Sound Chip (GI-AY-3-8910)
8000	R	D	D	D	D	D	D	D	D	Read from Sound Chip

Address Decoder

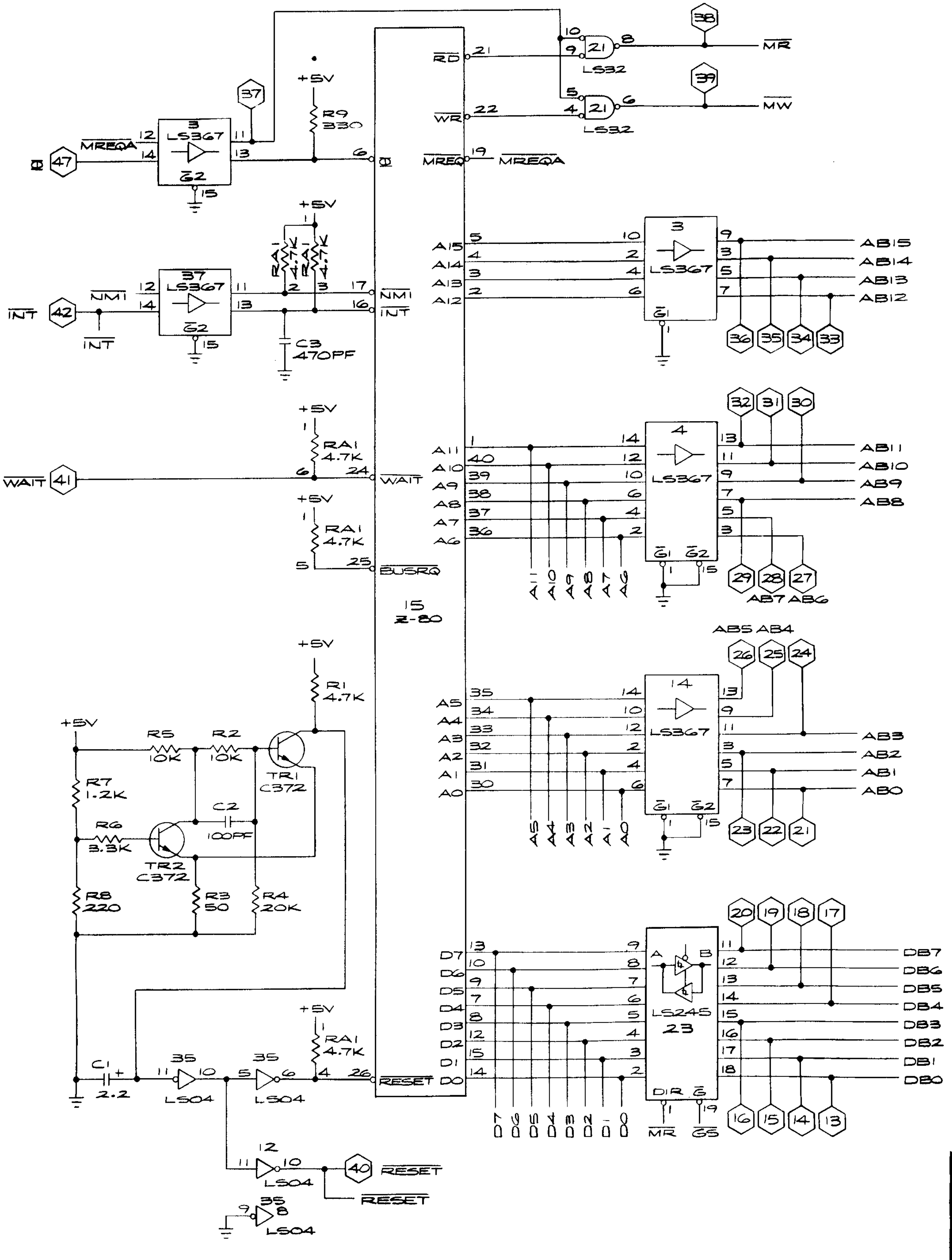


Kangaroo CPU PCB Schematic Diagram

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3rd printing

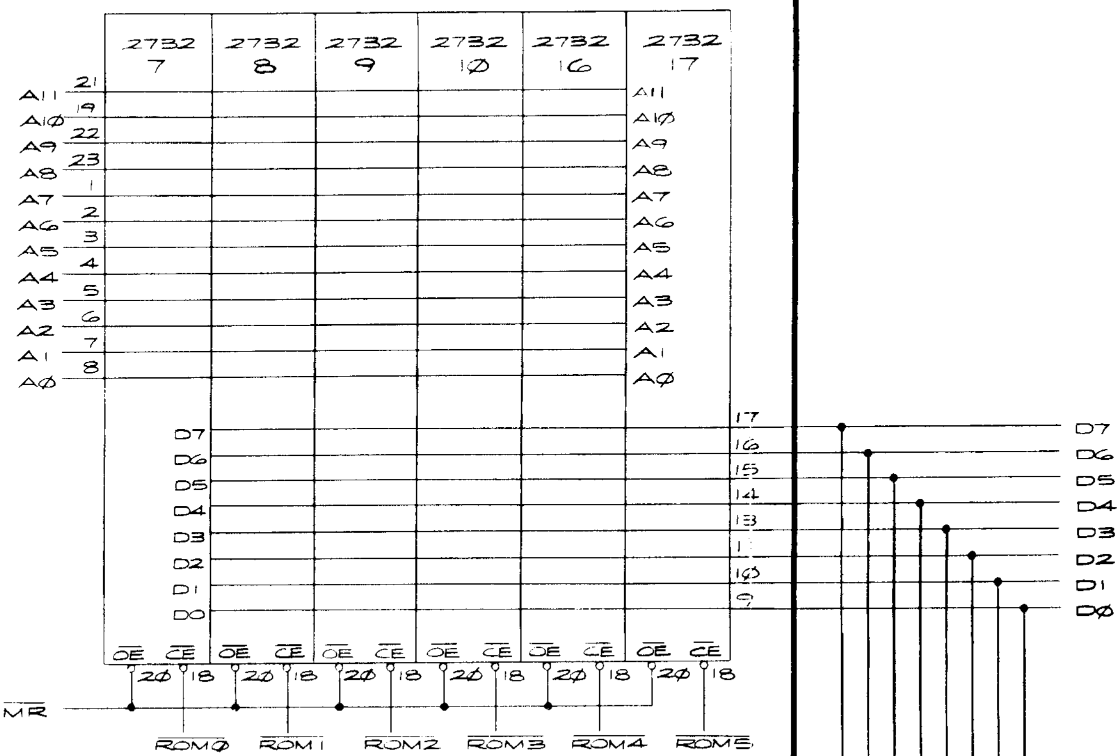
Game Microprocessor



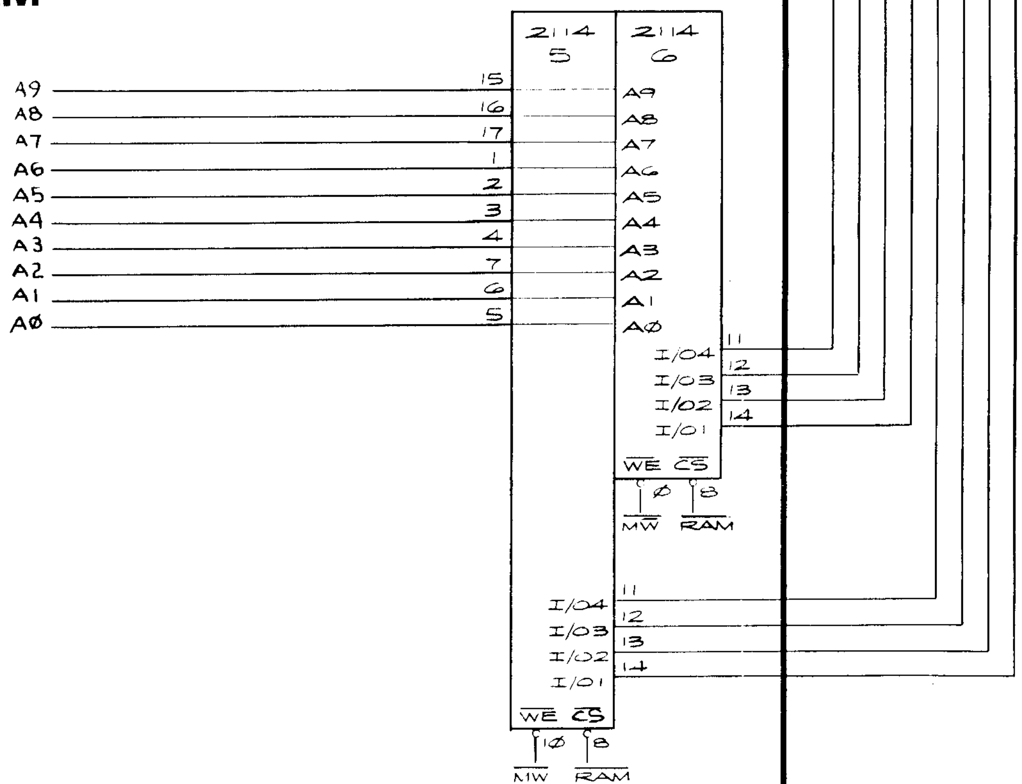
Kangaroo CPU PCB Schematic Diagram

SP-204 Sheet 5B
3rd printing

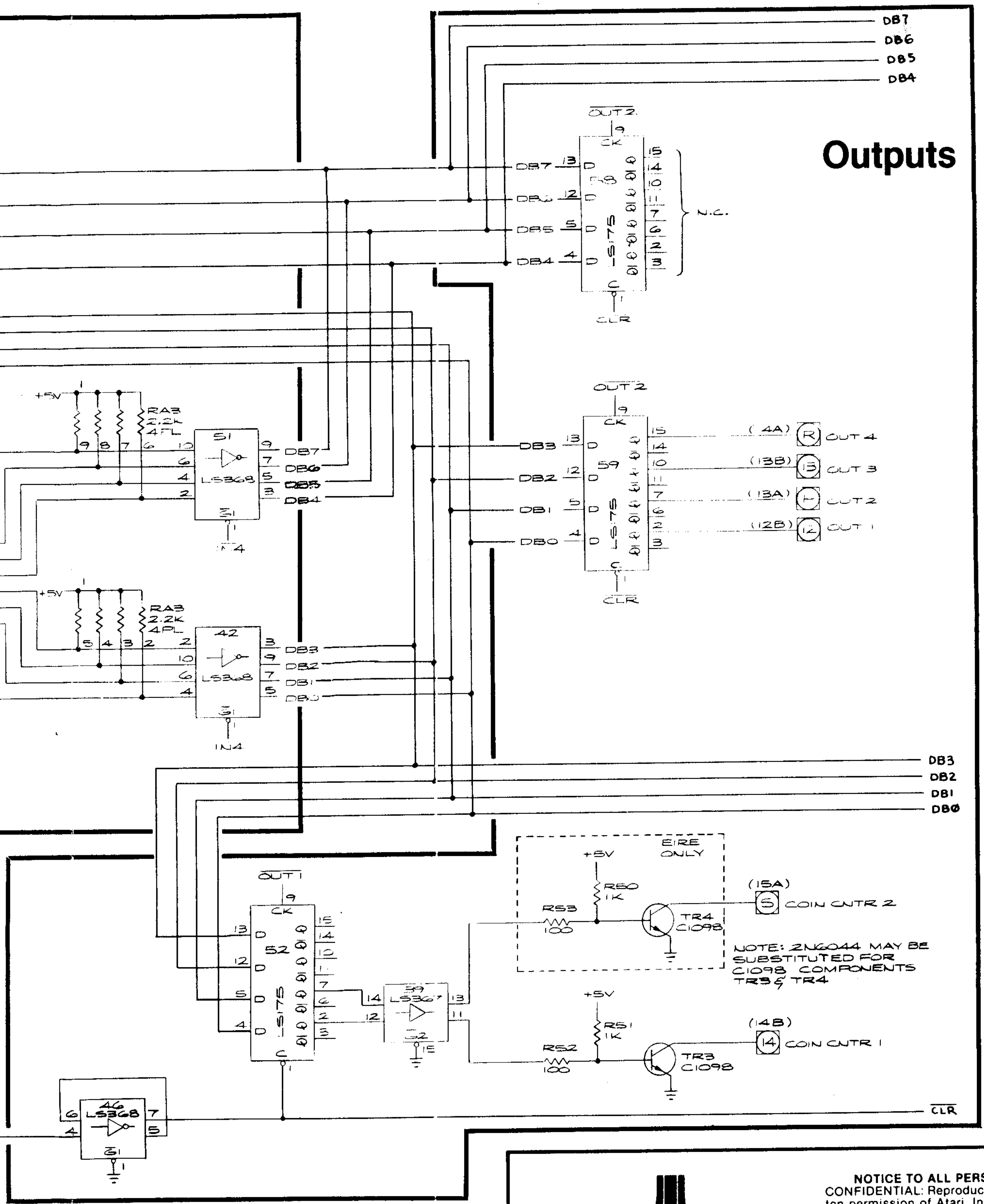
Program ROM



RAM



Outputs

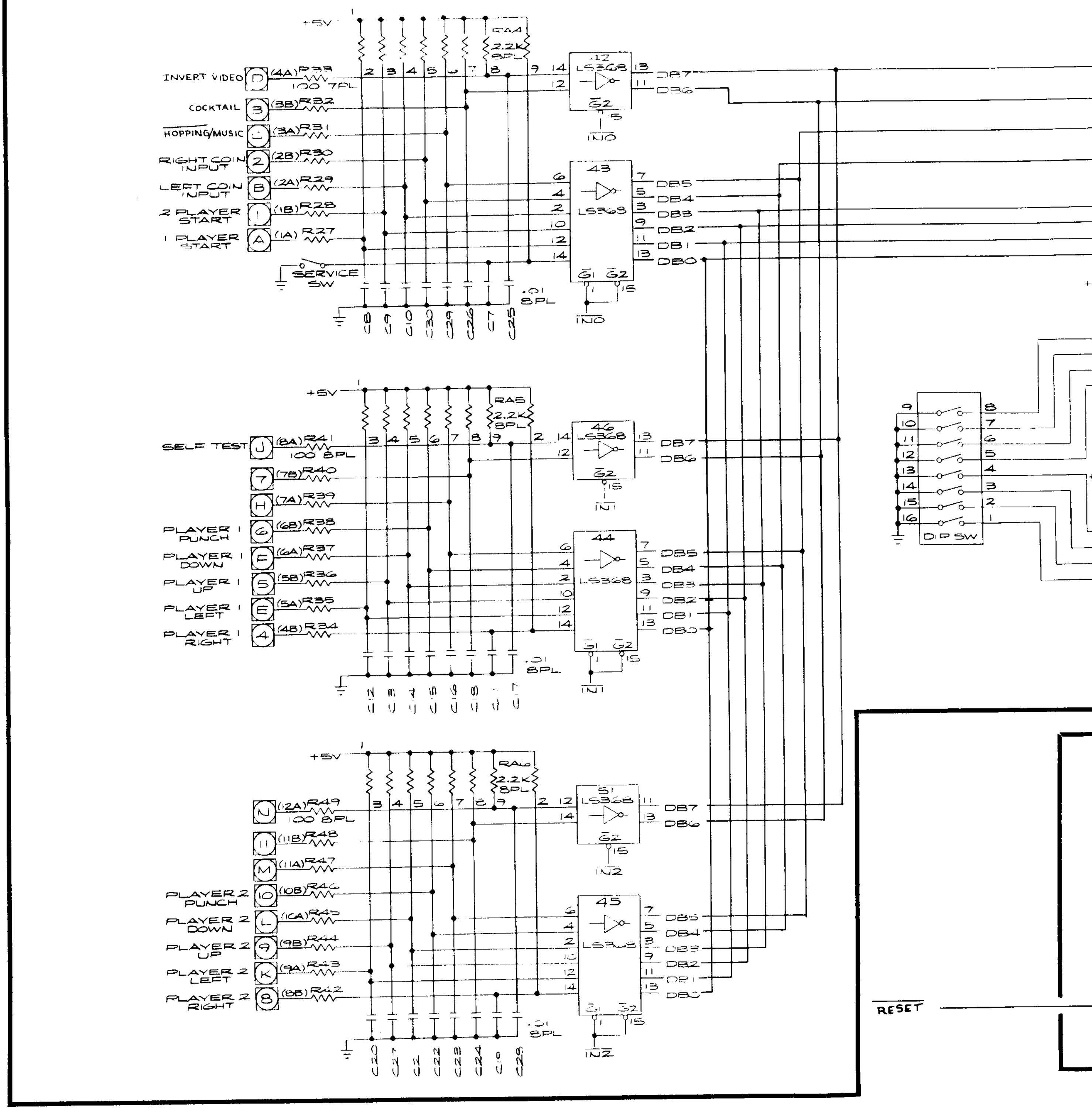


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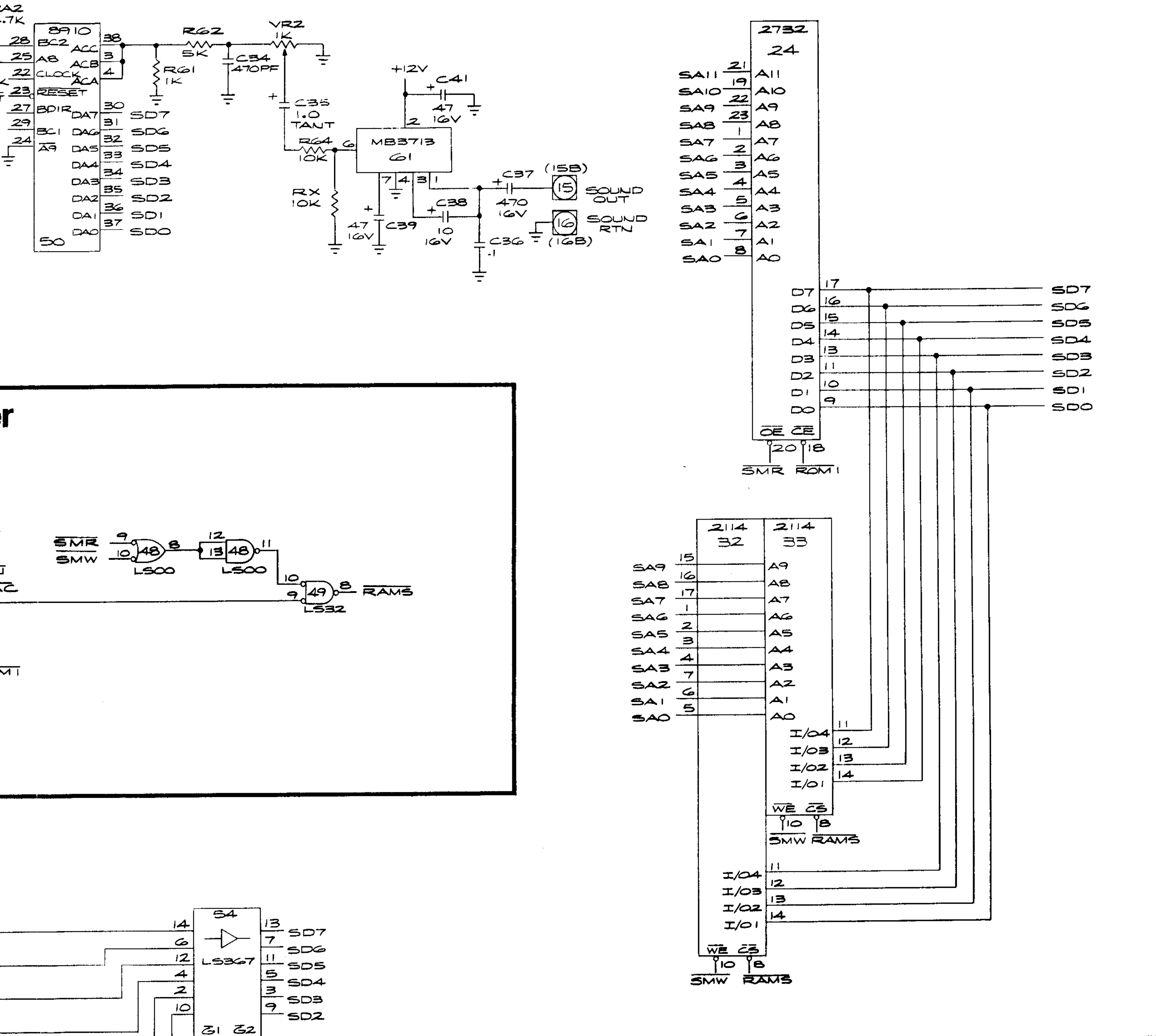
Kangaroo CPU PCB Schematic Diagram

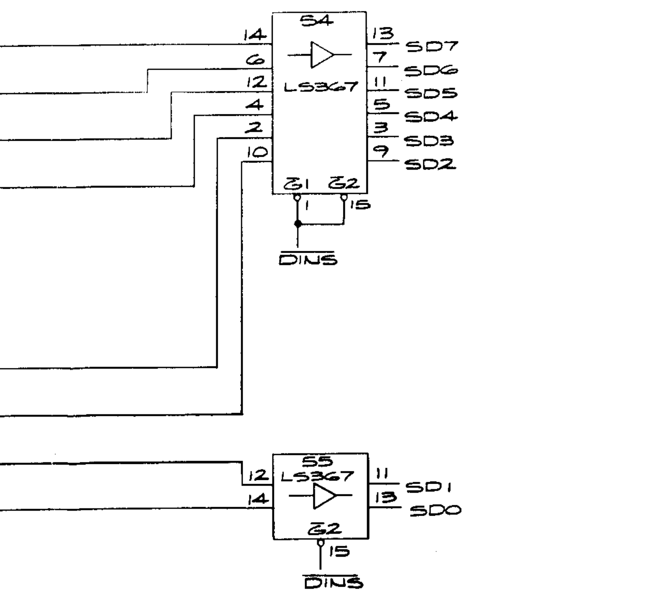
SP-204 Sheet 6A
3rd printing

Inputs



+5V
RA4 2.2K 8PL
INVERT VIDEO
COCKTAIL
HOPPING/MUSIC
RIGHT COIN INPUT
LEFT COIN INPUT
2 PLAYER START
1 PLAYER START
SERVICE SW
LS368
IN0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
.01 8PL
RA5 2.2K 8PL
SELF TEST
PLAYER 1 PUNCH
PLAYER 1 DOWN
PLAYER 1 UP
PLAYER 1 LEFT
PLAYER 1 RIGHT
IN1
RA6 2.2K 8PL
PLAYER 2 PUNCH
PLAYER 2 DOWN
PLAYER 2 UP
PLAYER 2 LEFT
PLAYER 2 RIGHT
IN2
DIP SW
RESET





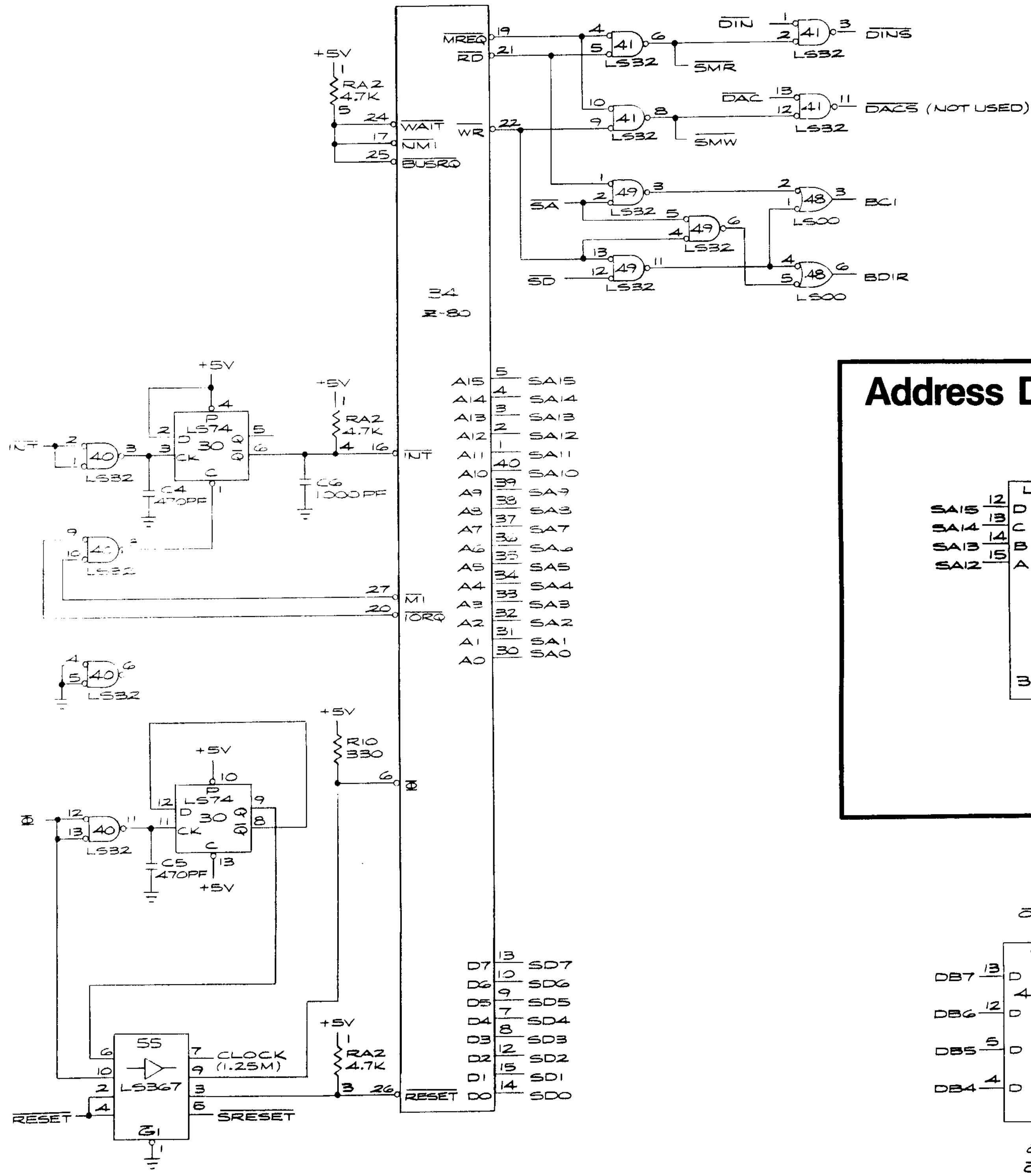
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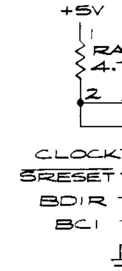
Kangaroo CPU PCB Schematic Diagram

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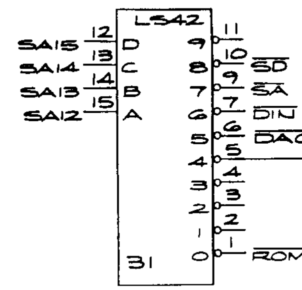
SP-204 Sheet 6B
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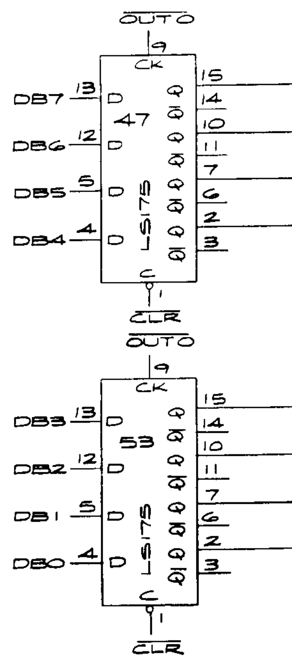
Sound Microprocessor

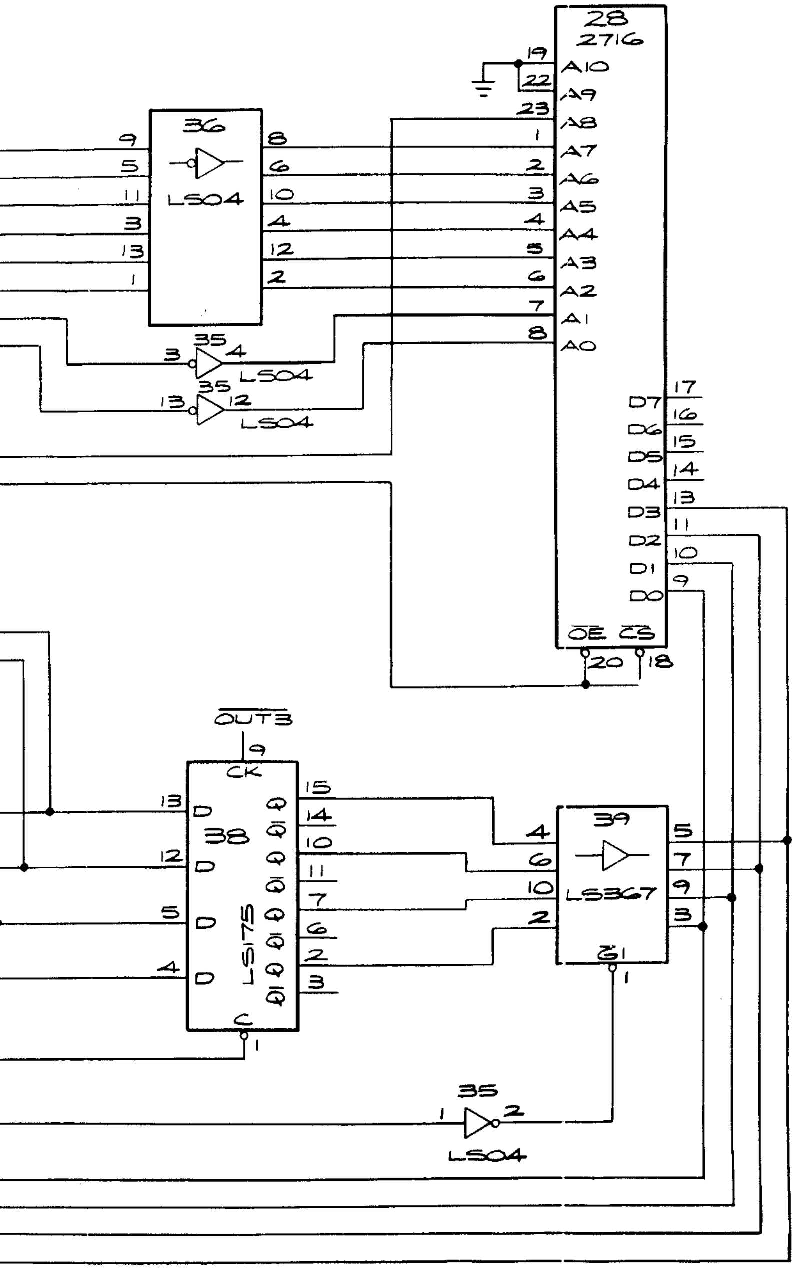




Address Decoder







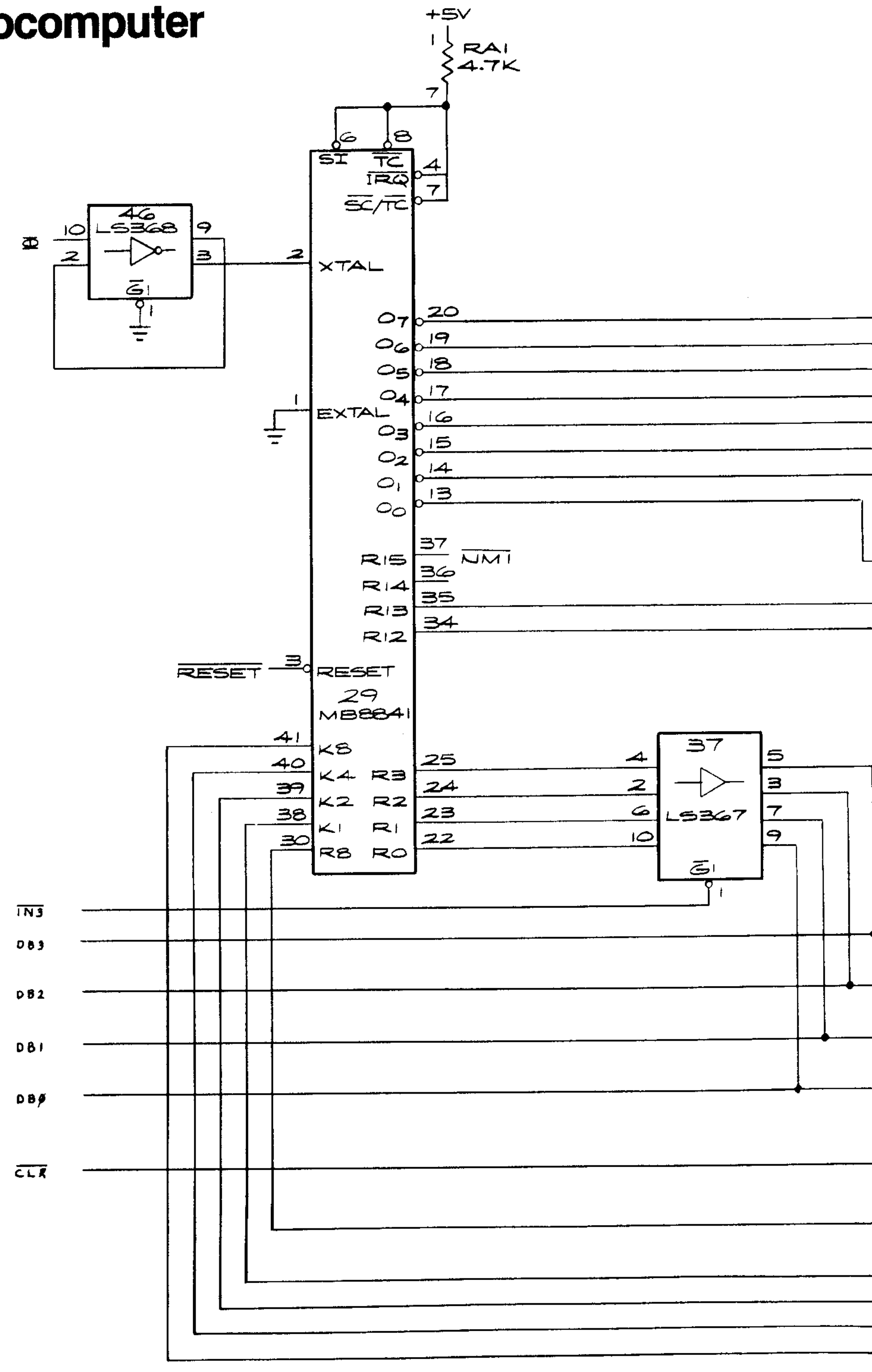
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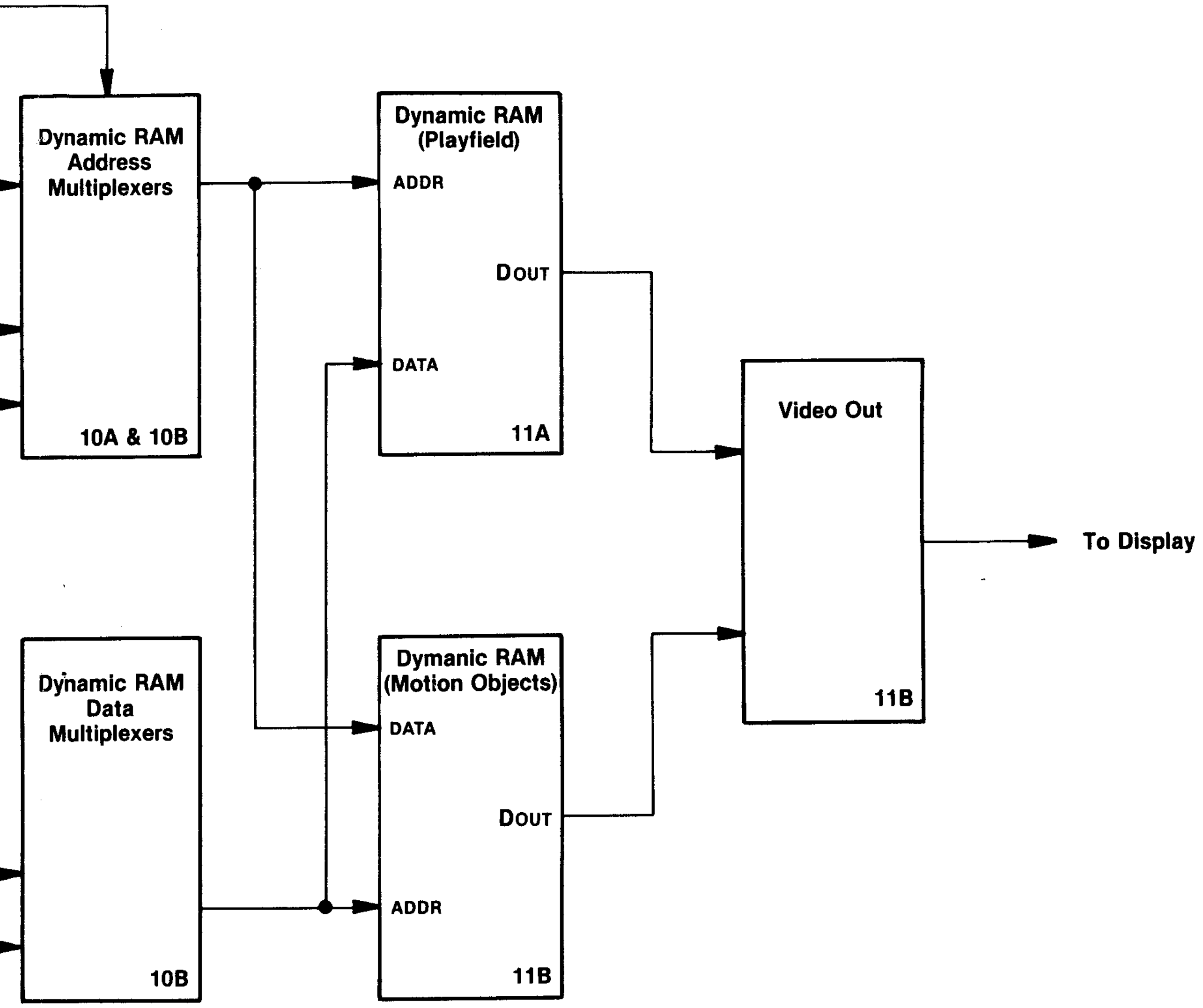
Kangaroo CPU PCB Schematic Diagram

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Custom Microcomputer

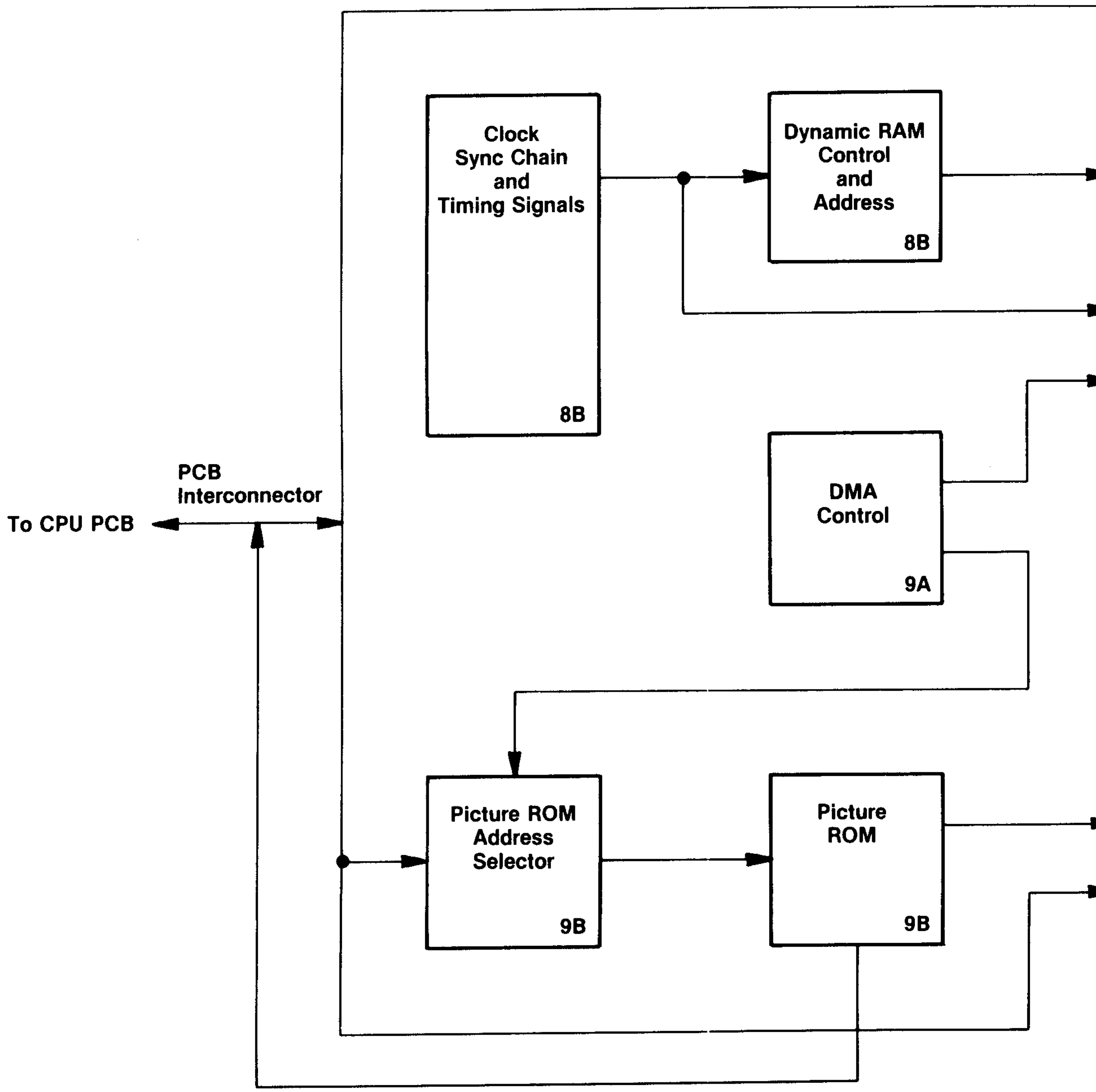




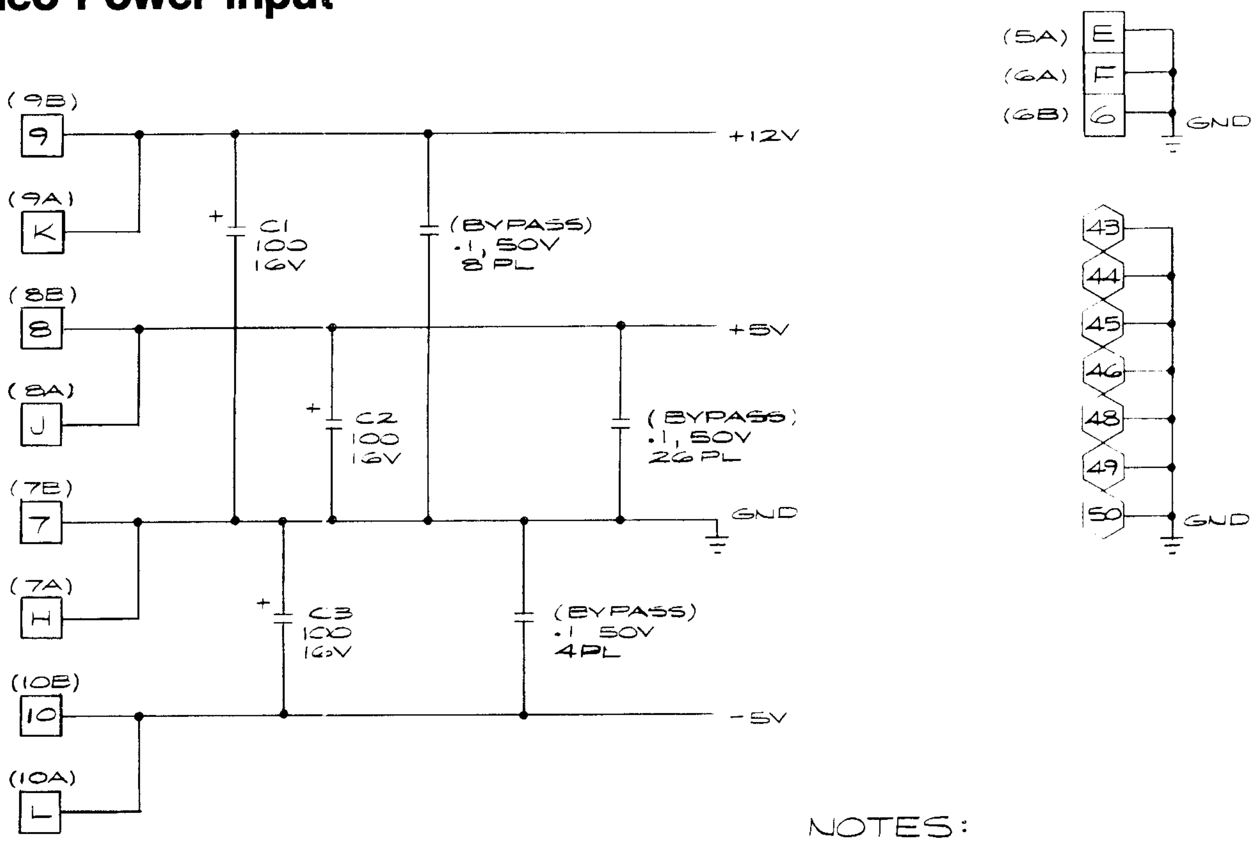
Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 7B
3rd printing

Block Diagram (Video PCB)



Video Power Input



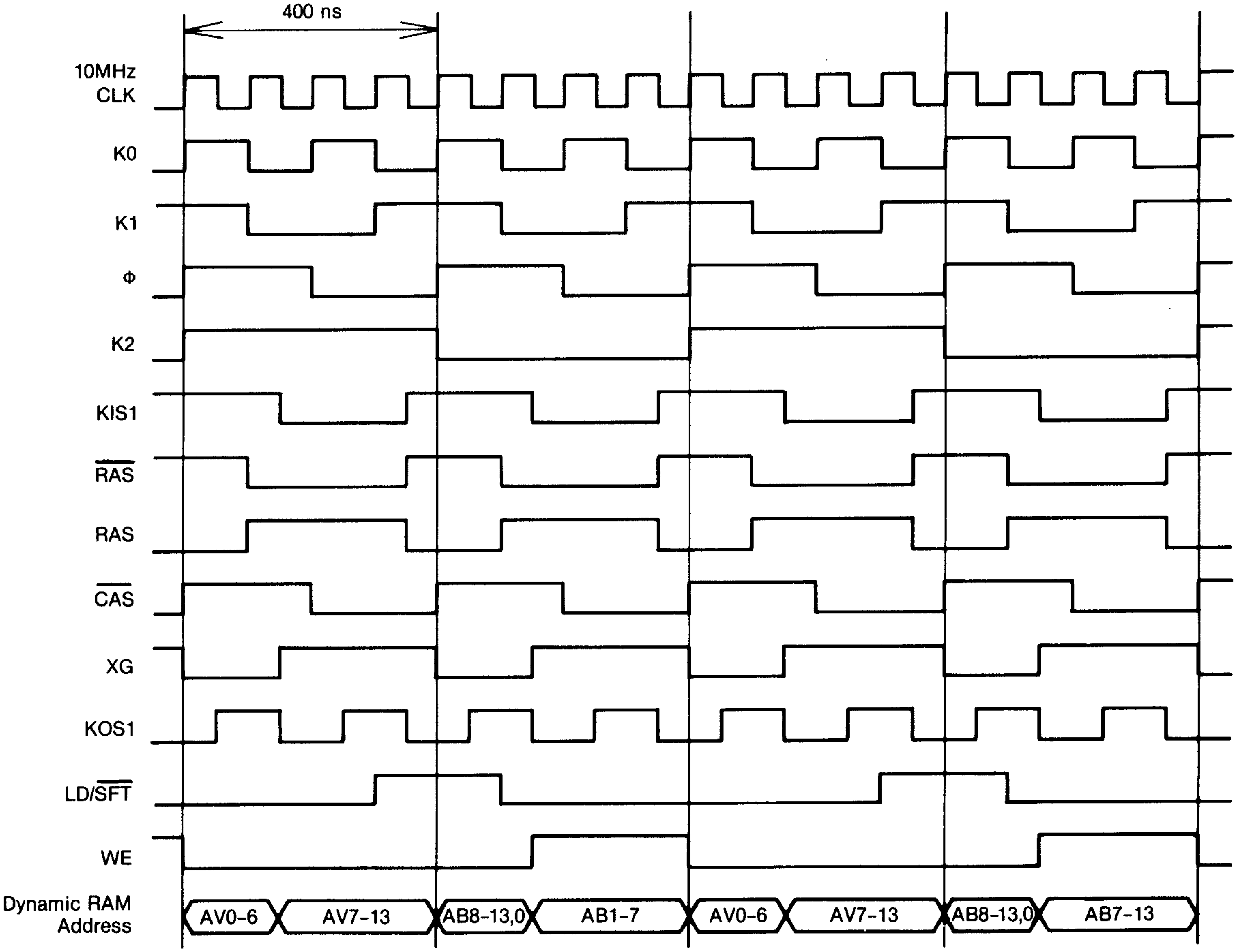
NOTES:

1. ⬡ = CONNECTOR CN1
2. □ = CONNECTOR CN4

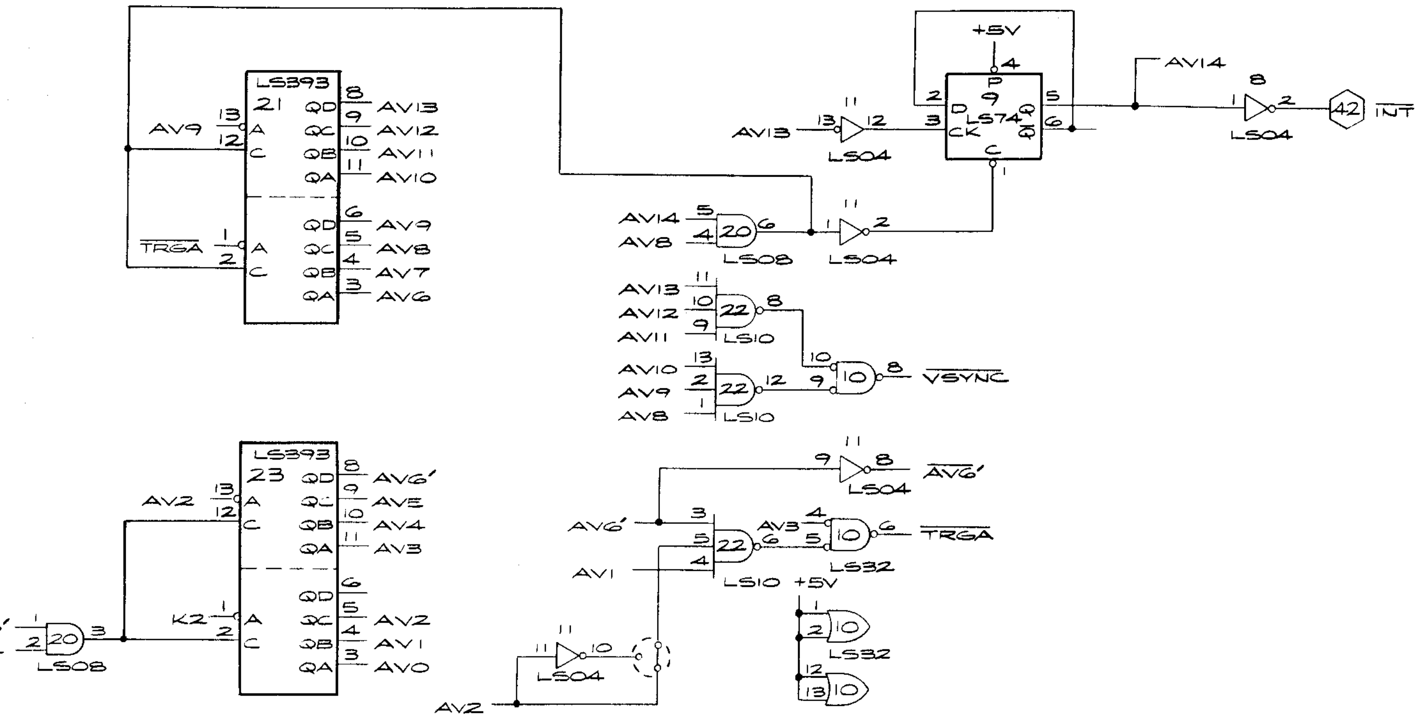
Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 8A
3rd printing

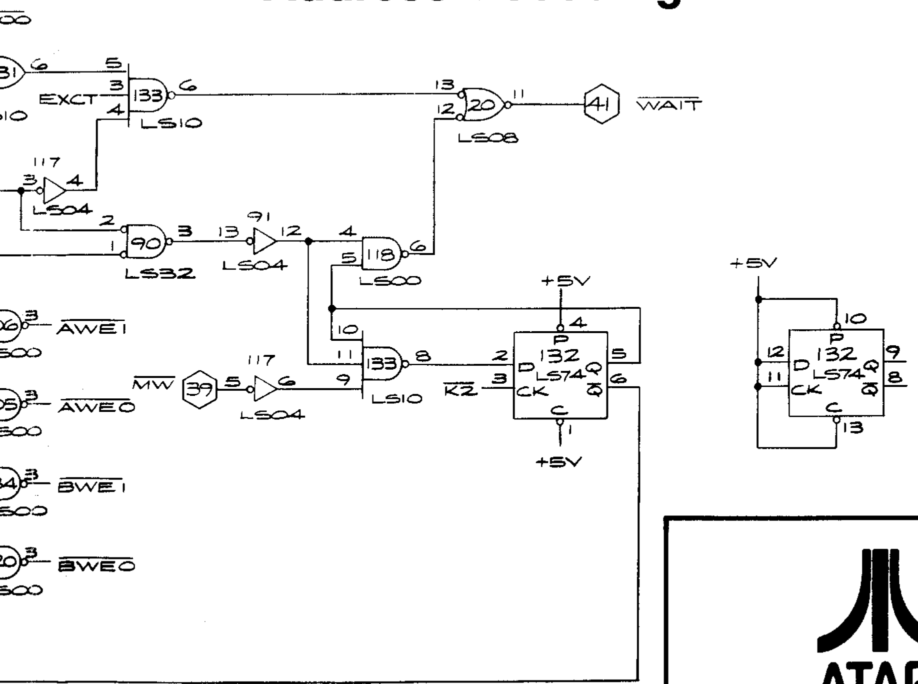
Dynamic RAM Timing Diagram (Video PCB)



nd Timing Signals



Address Decoding



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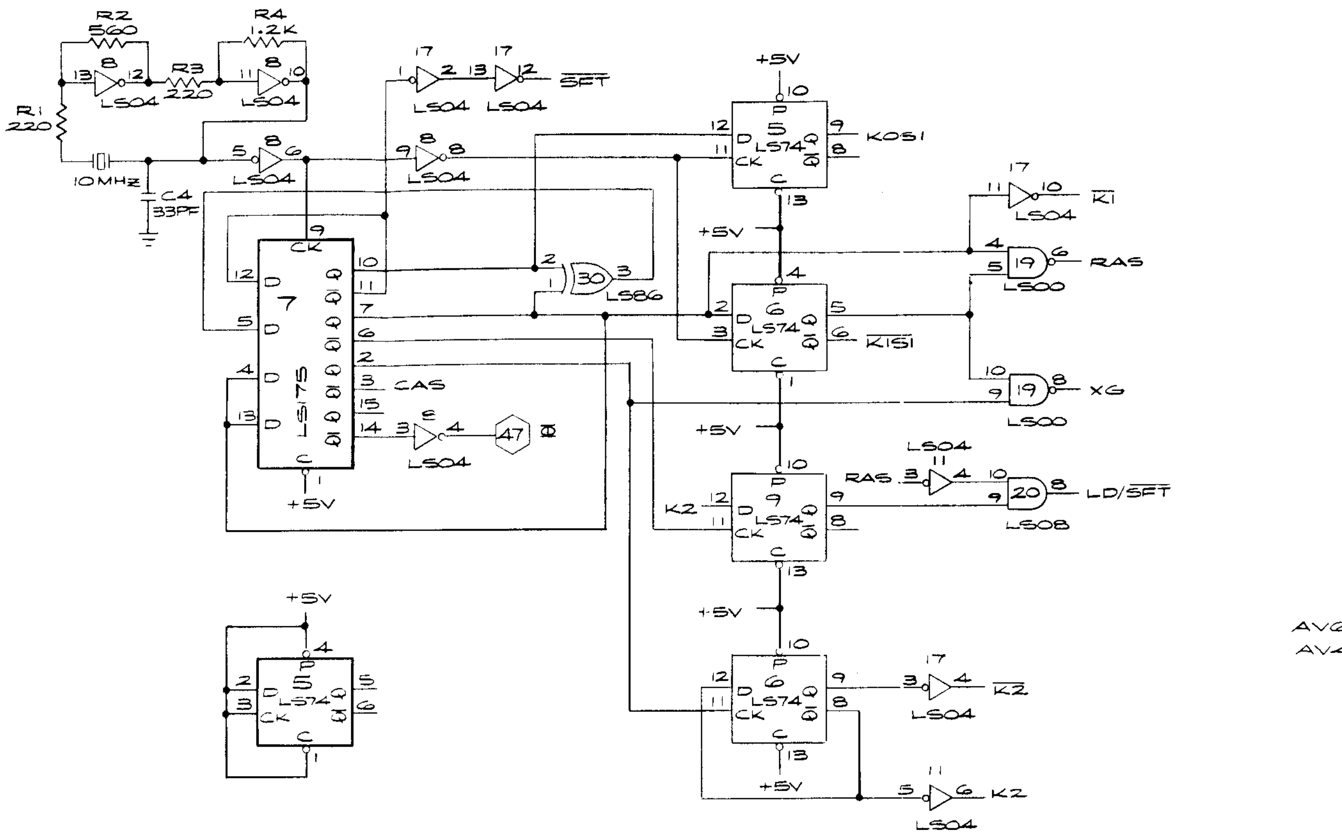
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Kangaroo Video PCB Schematic Diagram

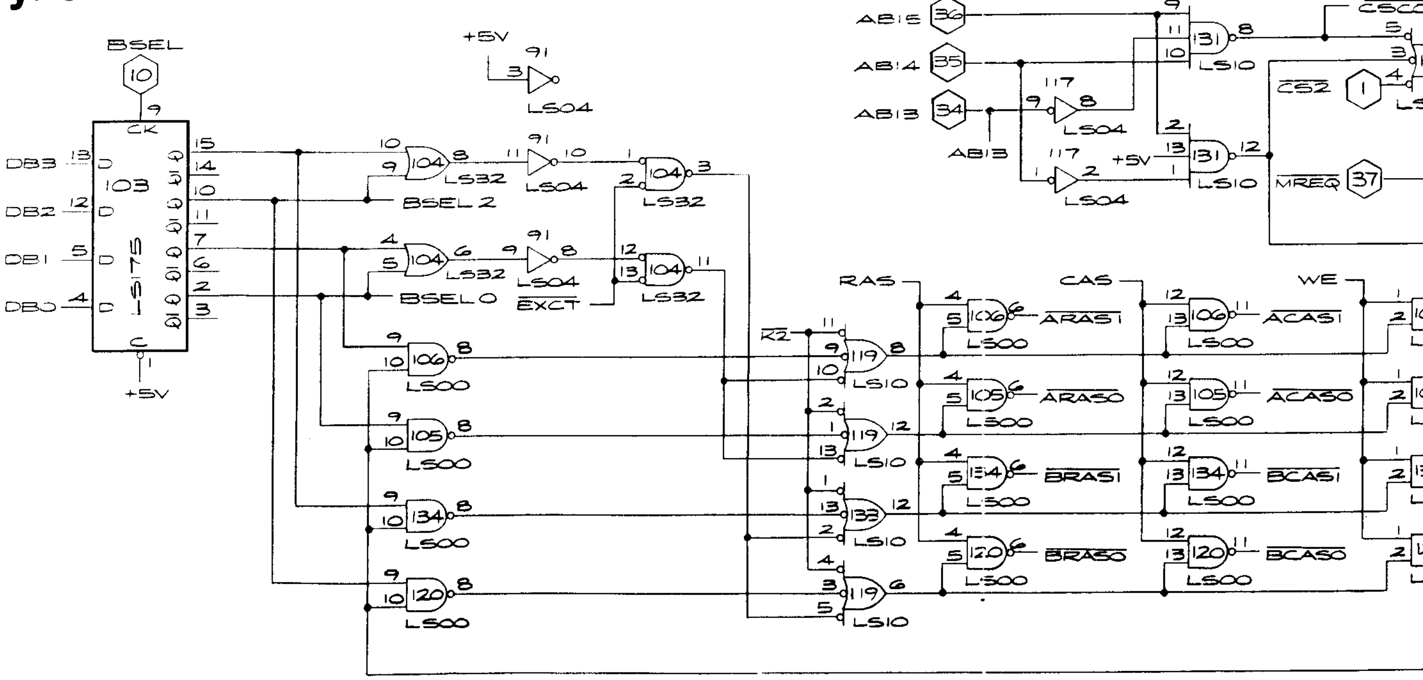
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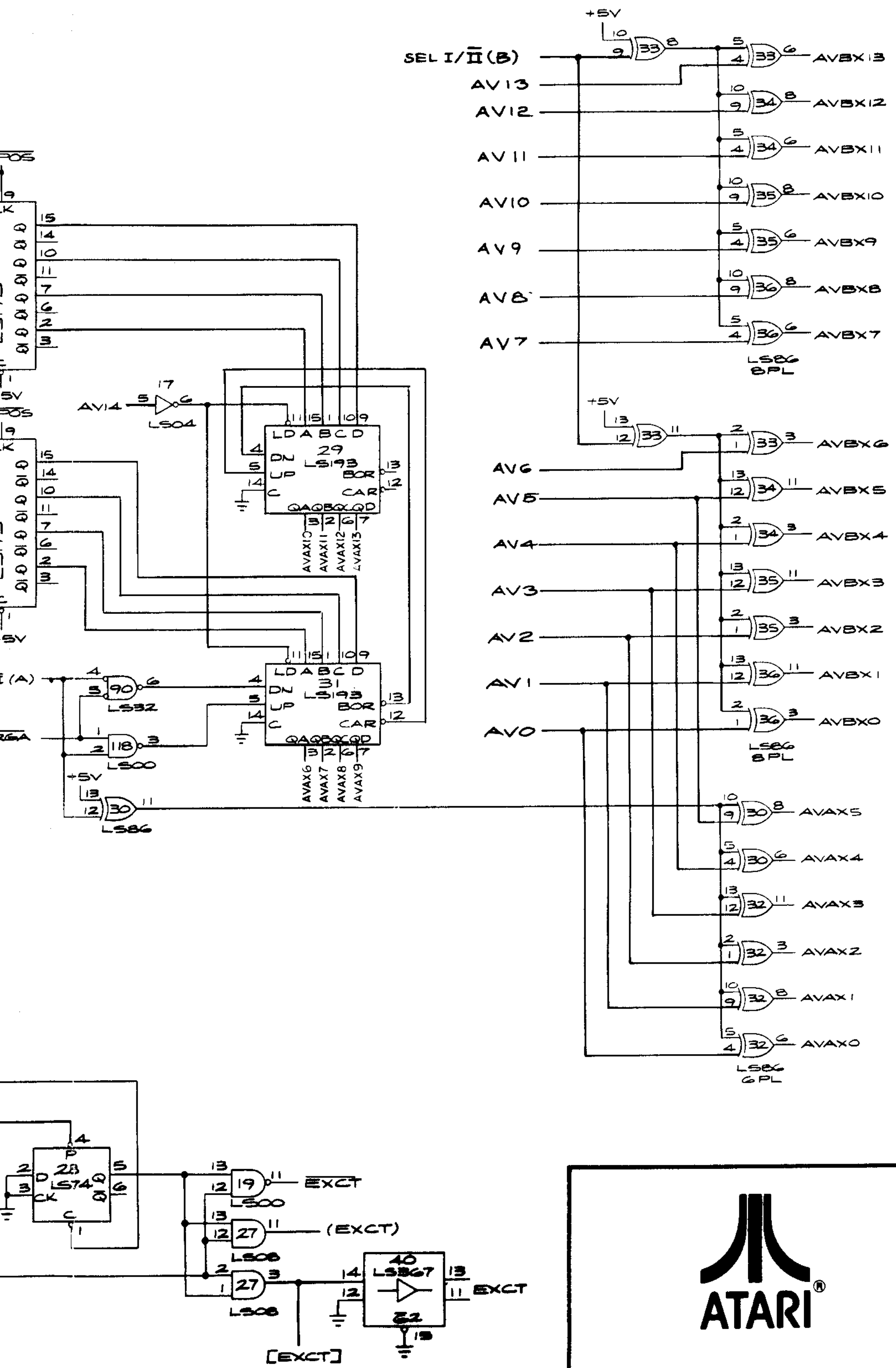
Clock, Sync Chain, a



Dynamic RAM Control



Dynamic RAM Video Address and Flip



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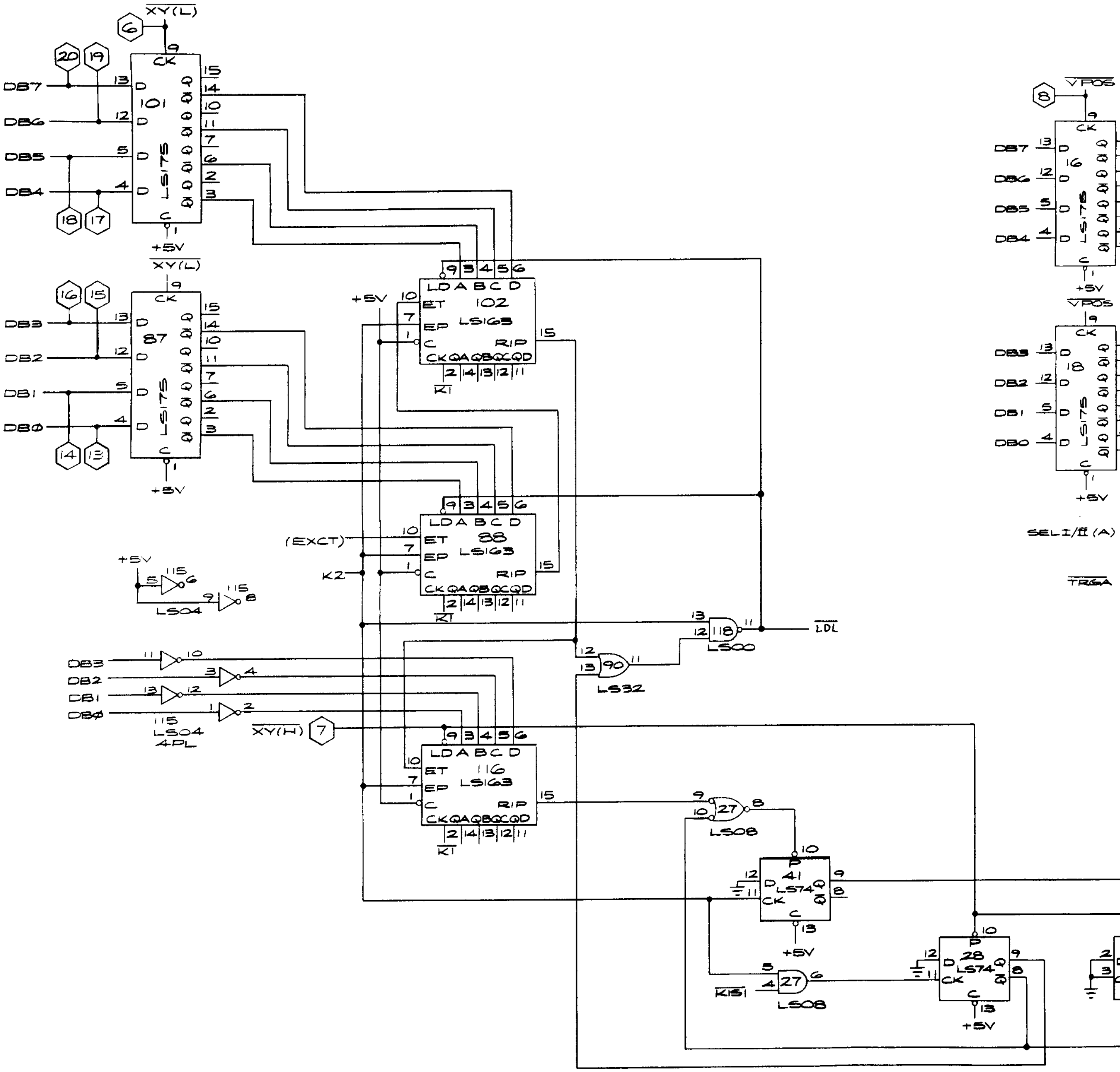
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Kangaroo Video PCB Schematic Diagram

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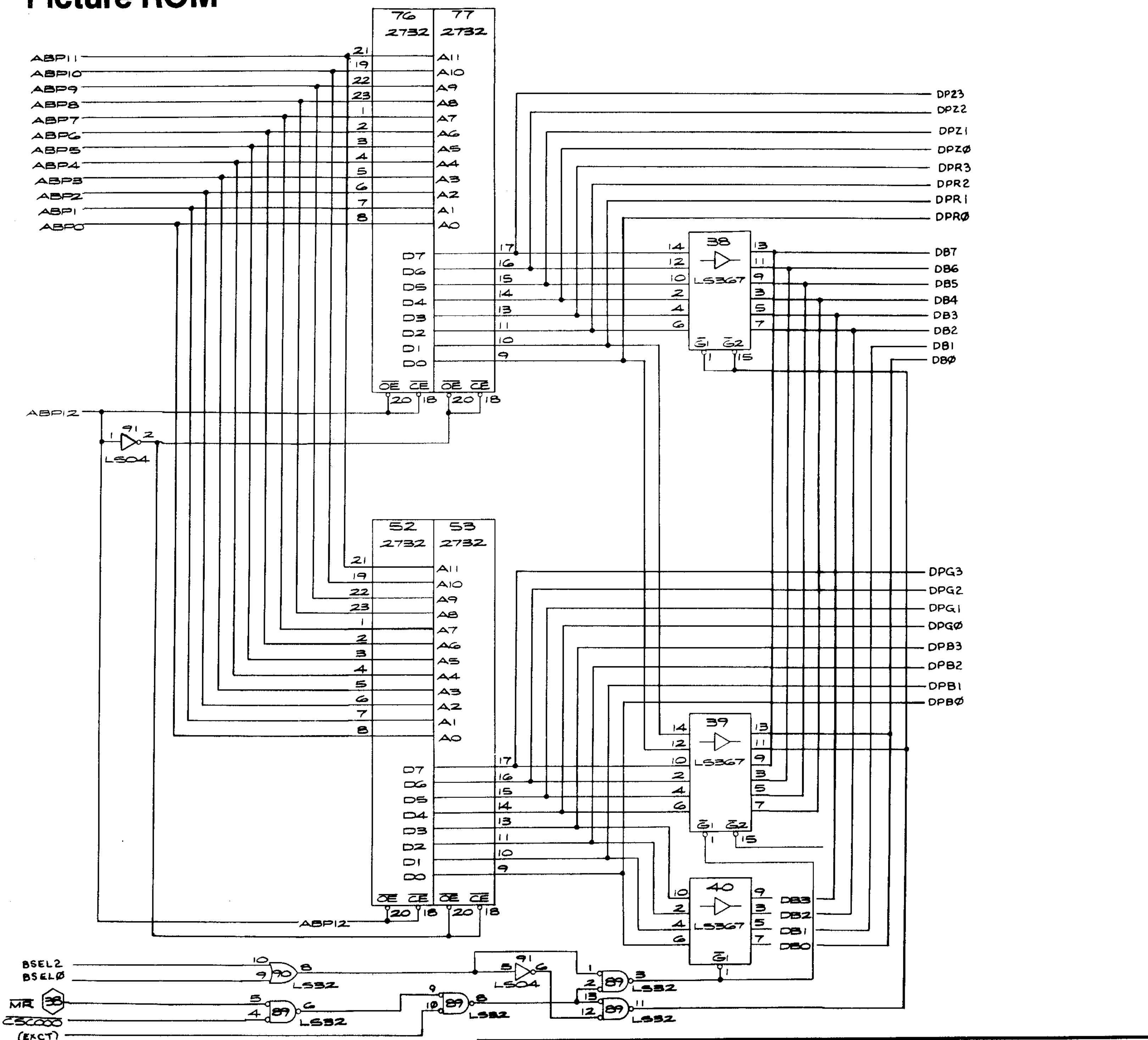
SP-204 Sheet 9A
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DMA Control



XY(L)
DB7
DB6
DB5
DB4
101
LS175
+5V
DB3
DB2
DB1
DBØ
87
LS175
102
LS163
88
LS163
116
LS163
(EXCT)
K2
K1
+5V
LS04
LS00
LDL
LS32
DB3
DB2
DB1
DBØ
115
LS04
4PL
XY(H)
LS08
41
LS74
28
LS74
K151
VPOS
DB7
DB6
DB5
DB4
16
LS175
DB3
DB2
DB1
DB0
18
LS175
SEL I/II (A)
TRGA

Picture ROM



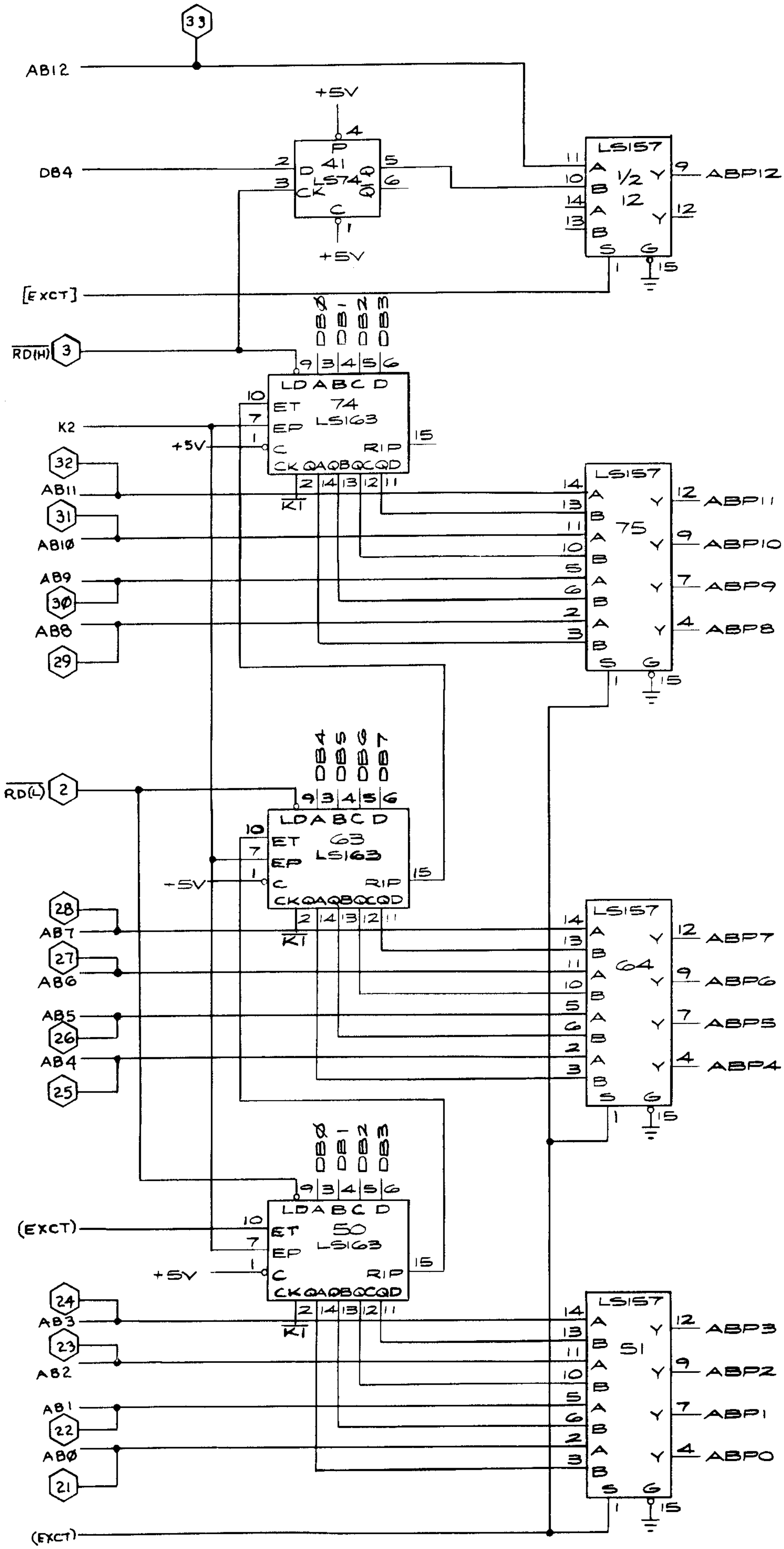
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ATARI®

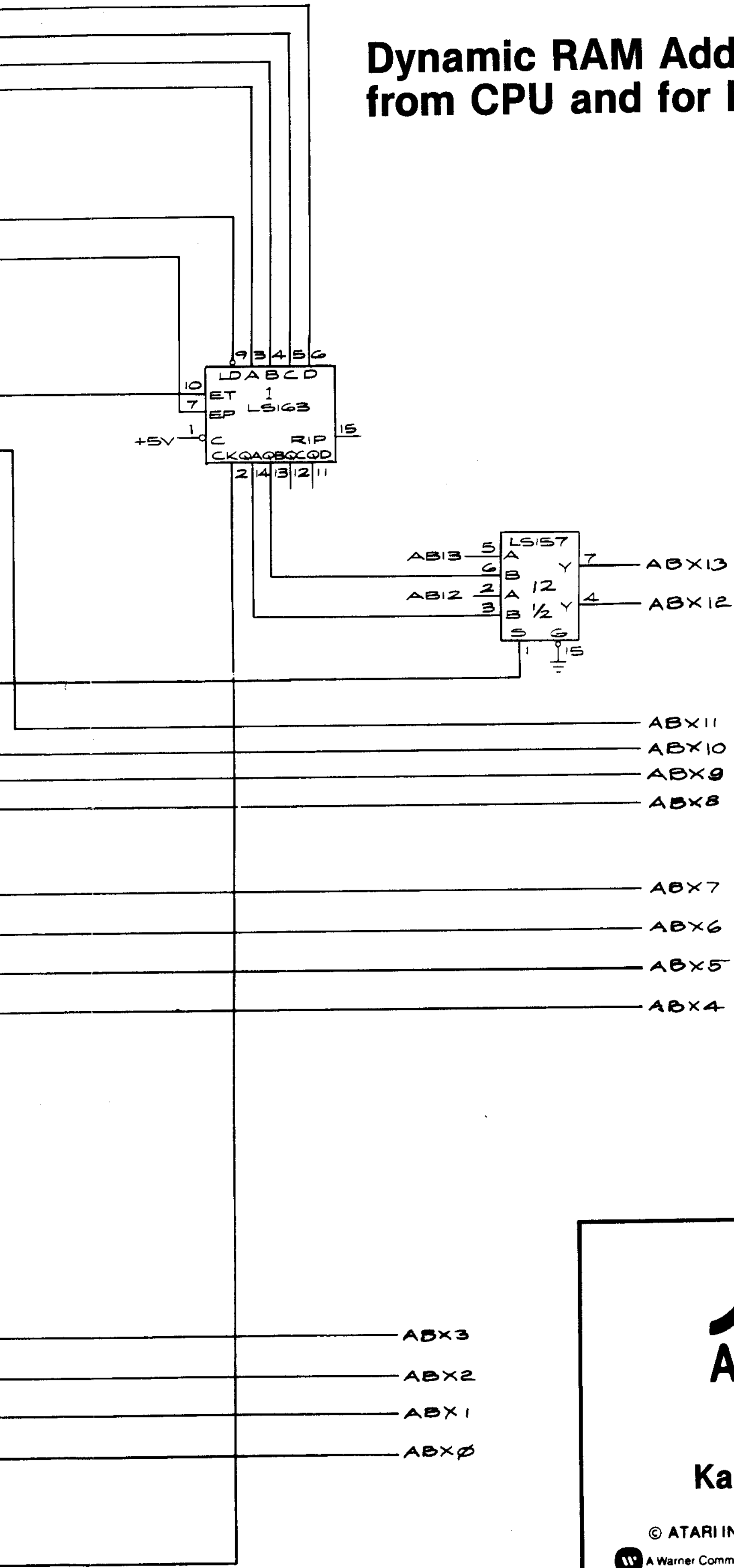
Kangaroo Video PCB Schematic Diagram

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Picture ROM Address Selector

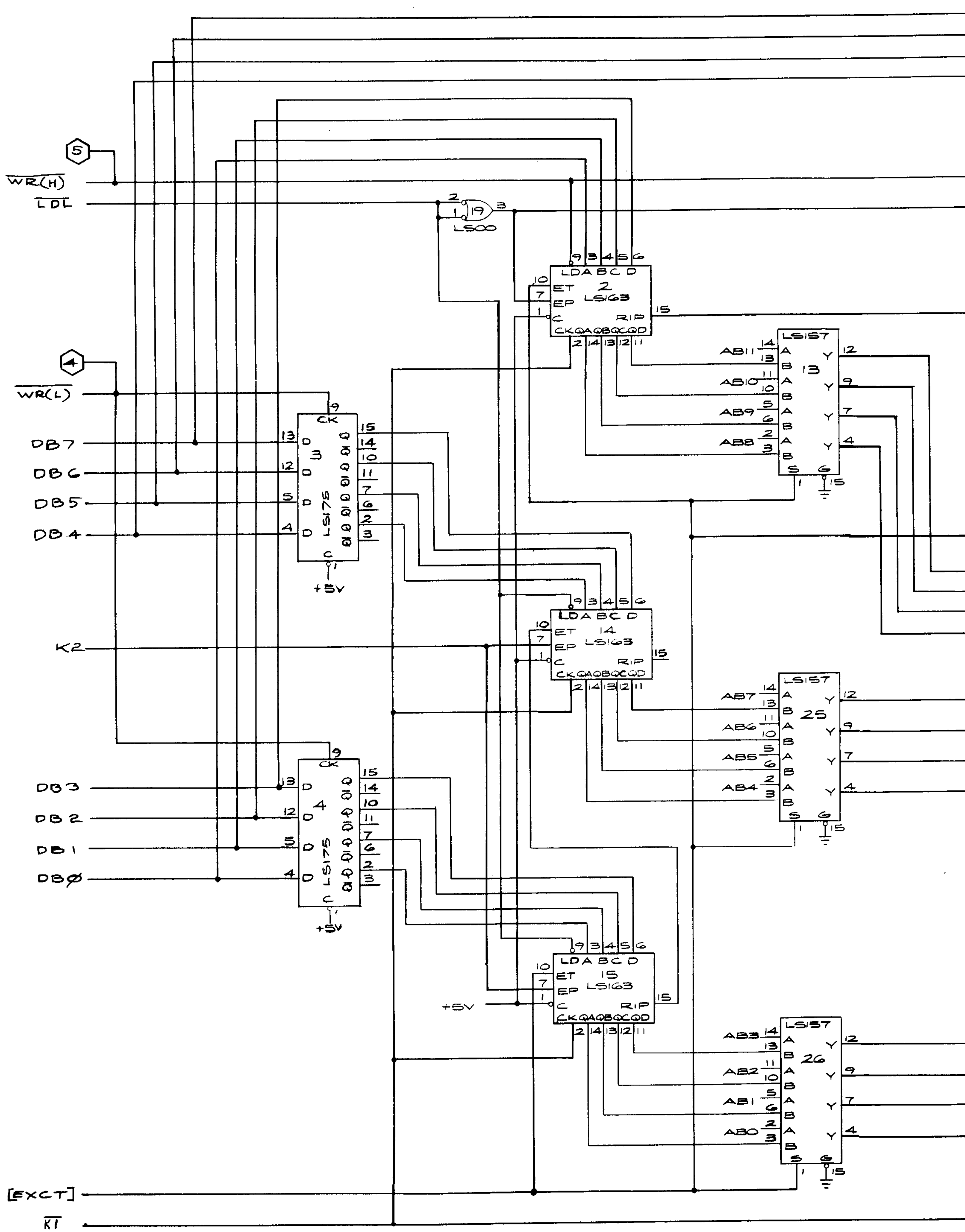


Dynamic RAM Address from CPU and for DMA

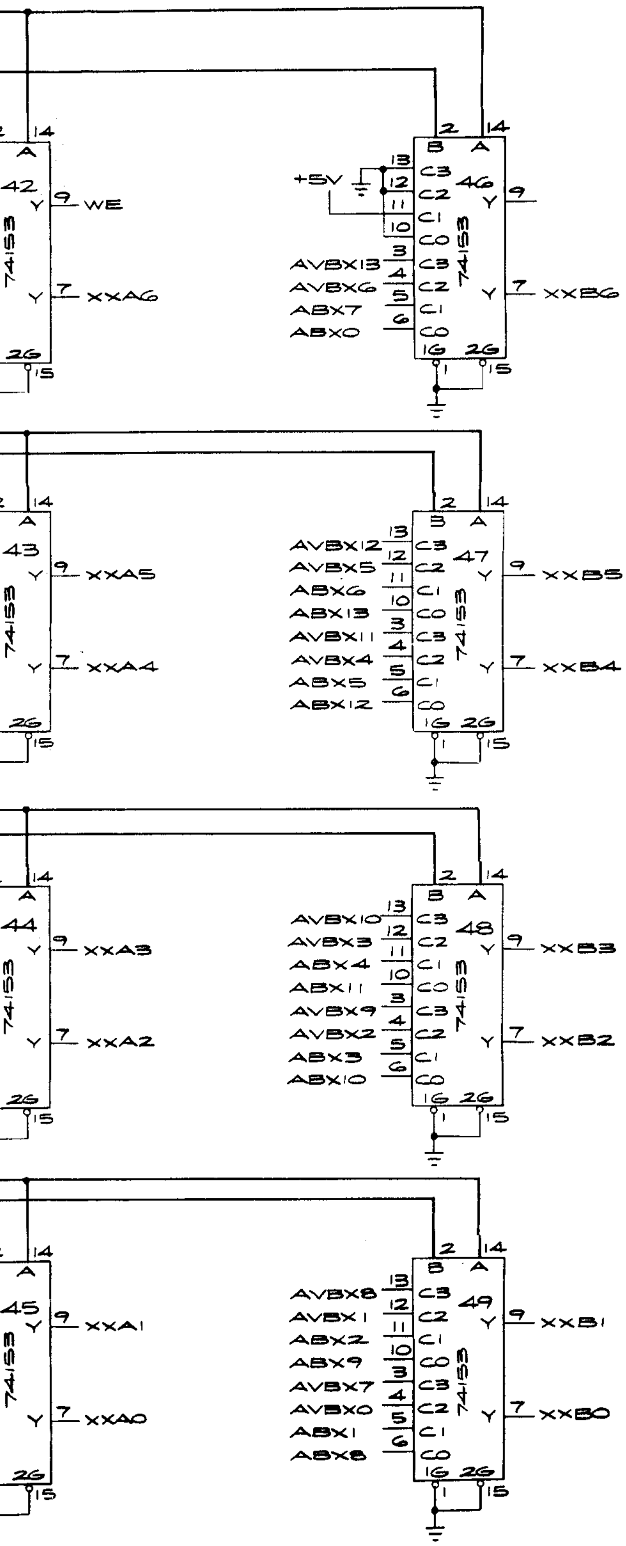


Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 10A
3rd printing


5
WR(H)
LDL
19
LS00
4
WR(L)
DB7
DB6
DB5
DB4
LS175
+5V
K2
DB3
DB2
DB1
DBØ
[EXCT]
KI
LDABCD
ET
EP
C
RIP
CKQAQBQCQD
2
LS163
14
LS163
15
LS163
LS157
13
AB11
AB10
AB9
AB8
LS157
25
AB7
AB6
AB5
AB4
LS157
26
AB3
AB2
AB1
AB0

Address Selector

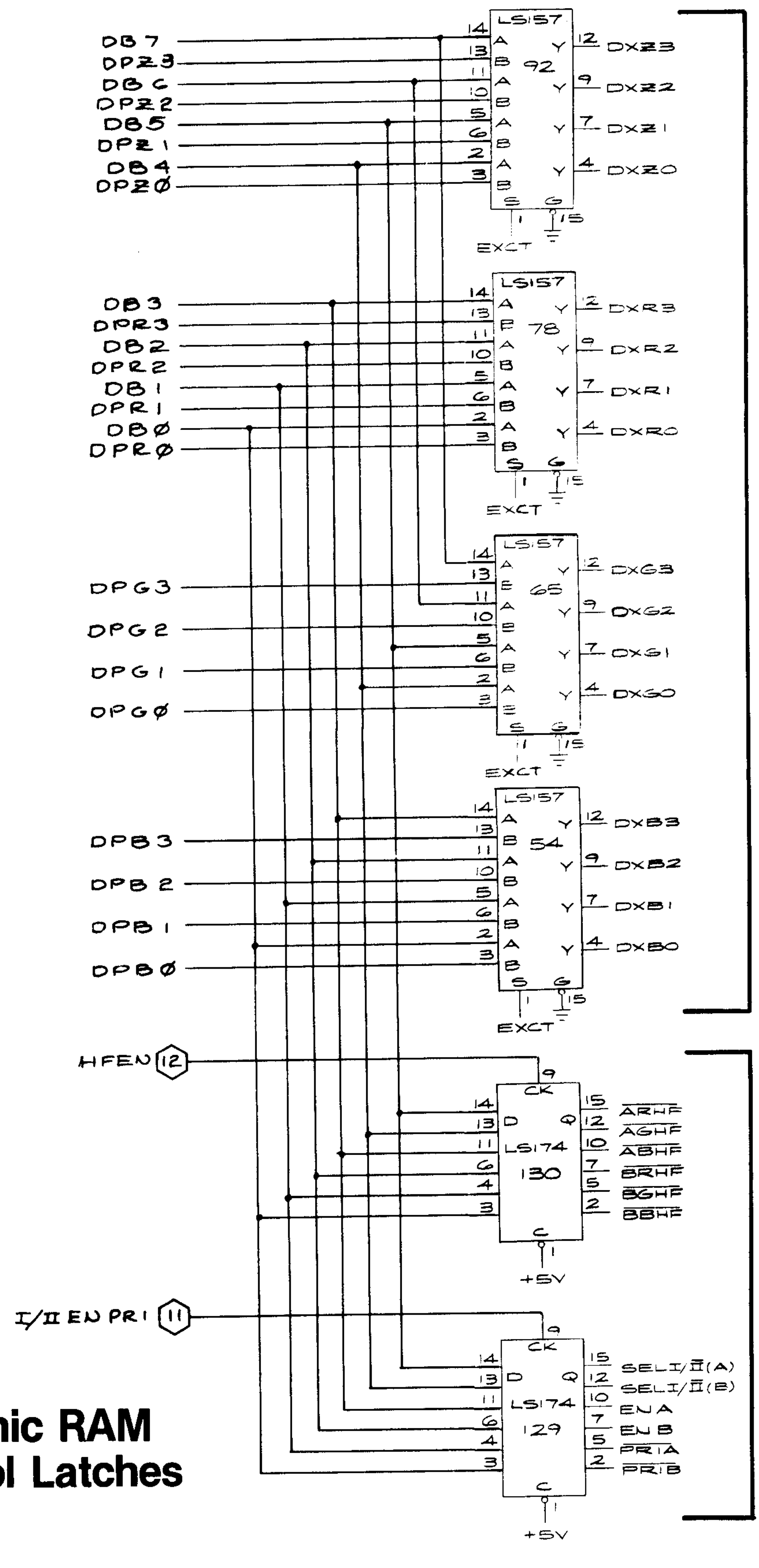


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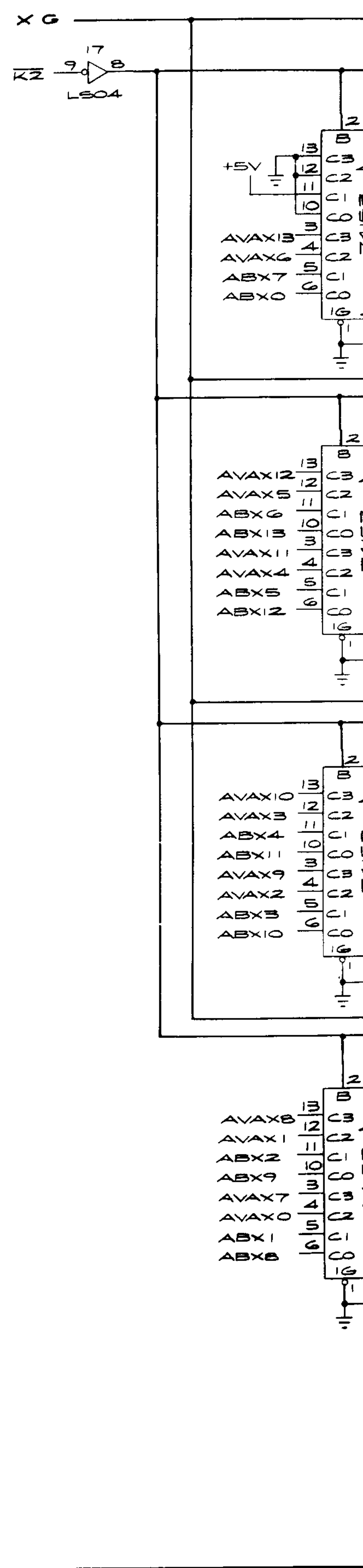
SP-204 Sheet 10B
3rd printing

Dynamic RAM Data Selector

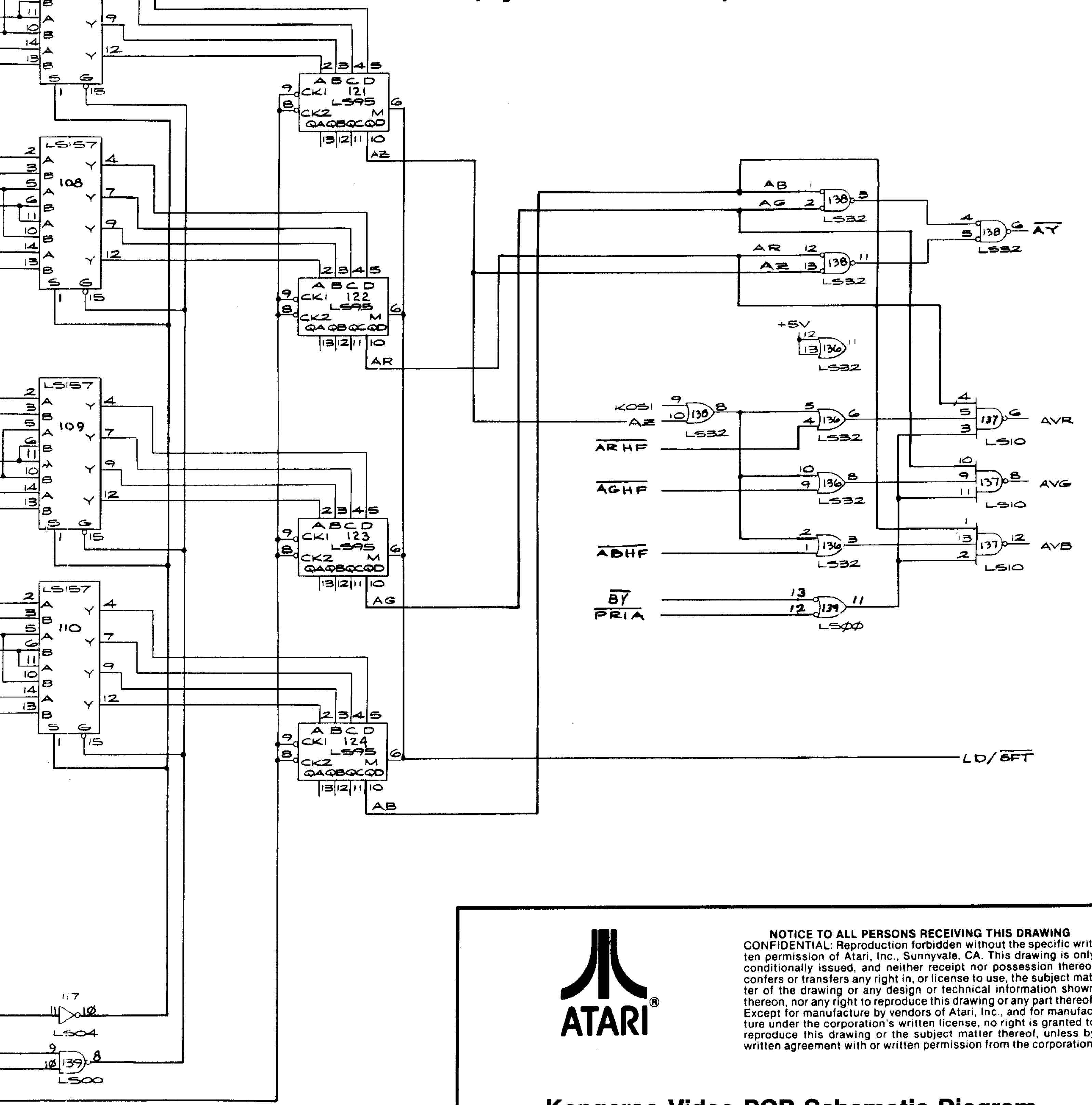


Dynamic RAM Control Latches

Dynamic RAM



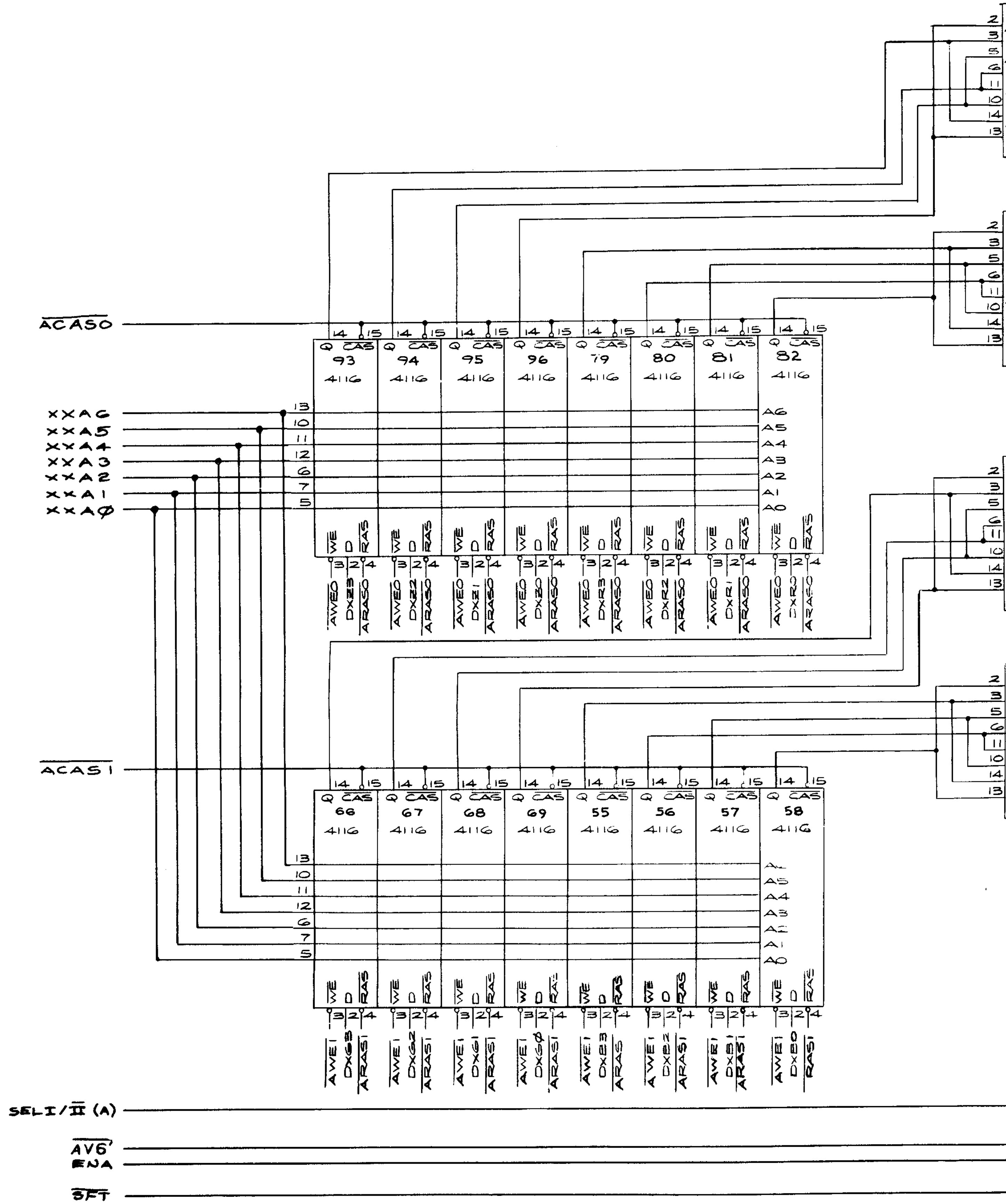
Playfield (Dynamic RAM A)



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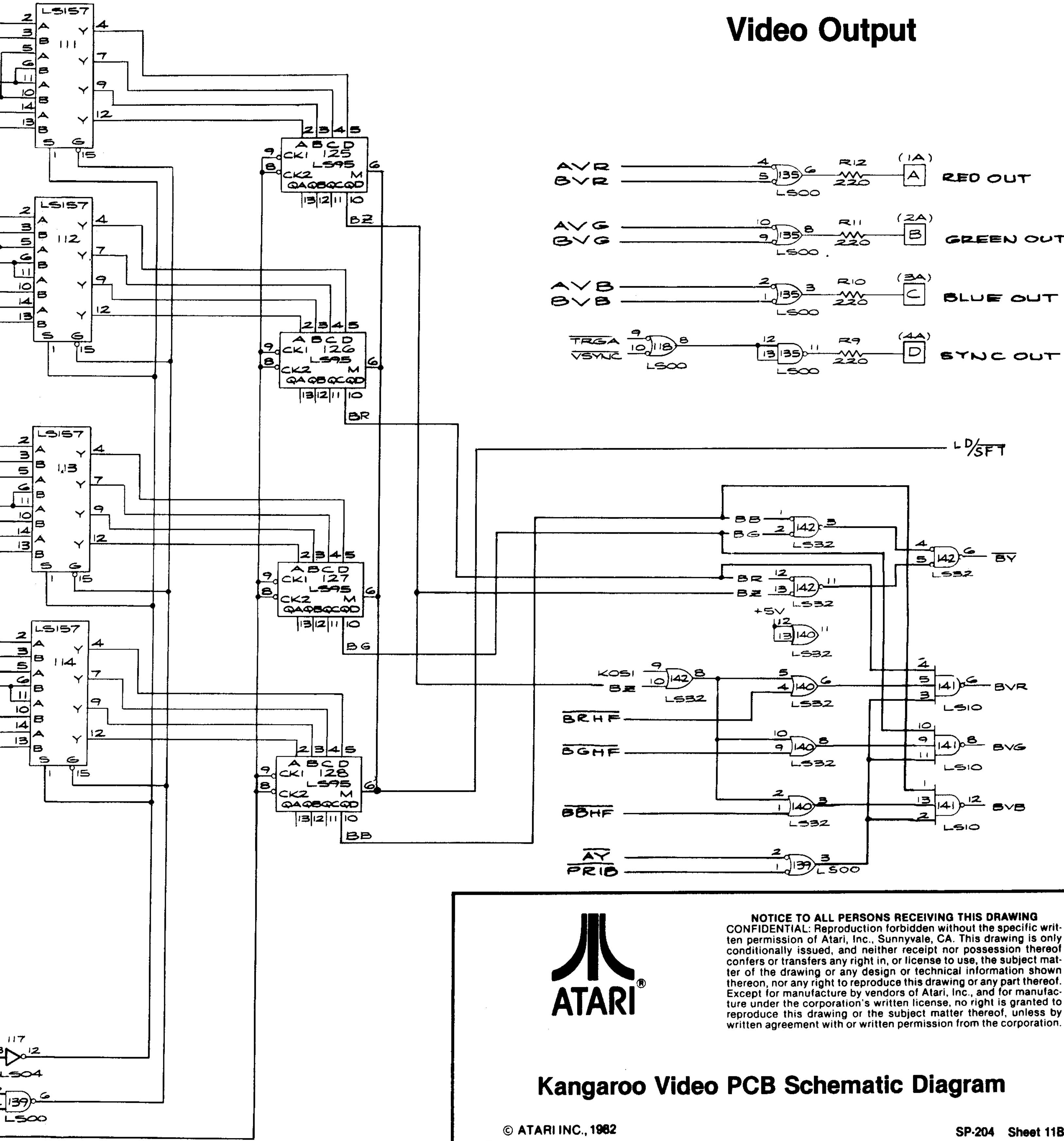
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SP-204 Sheet 11A
3rd printing



ACAS0
ACAS1
XXA6
XXA5
XXA4
XXA3
XXA2
XXA1
XXAØ
93 94 95 96 79 80 81 82
66 67 68 69 55 56 57 58
4116
Q CAS
WE D RAS
A6 A5 A4 A3 A2 A1 A0
AWE0 DXZ3 ARAS0
AWE0 DXZ2 ARAS0
AWE0 DXZ1 ARAS0
AWE0 DXZ0 ARAS0
AWE0 DXR3 ARAS0
AWE0 DXR2 ARAS0
AWE0 DXR1 ARAS0
AWE0 DXR0 ARAS0
AWE1 DXG3 ARAS1
AWE1 DXG2 ARAS1
AWE1 DXG1 ARAS1
AWE1 DXGØ ARAS1
AWE1 DXB3 ARAS
AWE1 DXB2 ARAS1
AWE1 DXB1 ARAS1
AWE1 DXB0 RAS1
SELI/II (A)
AV6'
ENA
SFT

Video Output



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Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 11B
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Motion Object (Dynamic RAM B)

